Gracias a la memoria se da en los hombres lo que se llama experiencia.

Aristóteles *(384 AC-322 AC) Filósofo griego*

	Actividad	Puntos	Fecha límite
PF6	Solución del examen	F	*Miércoles 8 de octubre*
PF7	Diseño Combinacional con HDL	F	*Viernes 10 de octubre*
PF8	Multiplexor	5	*Miércoles 15 de octubre*
AF3	Decodificador con Display	10	*Lunes 18 de octubre*
PF9	Flip Flops	F	*Lunes 27 de octubre*
PF10	Pulsos de sincronía	5	*Viernes 7 de noviembre*
AF4	Diseño Secuencial	10	
AF5	PIA	40	Día del examen

Flip Flops
Circuitos lógicos secuenciales

Origen etimológico

- **“Flip”** significa “voltear” o “cambiar rápidamente”.
- **“Flop”** representa el retorno o cambio contrario.

Juntas, las palabras **“flip-flop”** evocan un movimiento de **ida y vuelta**, exactamente como el circuito cambia entre los estados lógicos **0 y 1**

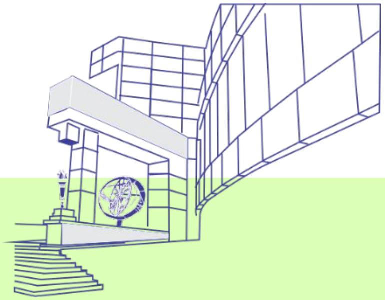
Flip Flops

Circuitos lógicos secuenciales

Son componentes fundamentales en el diseño de sistemas secuenciales debido a su capacidad de almacenar información.

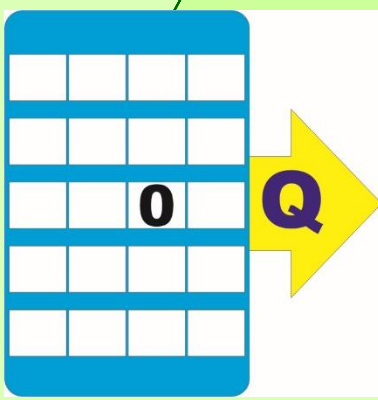
También se les conoce con varios nombres, como:

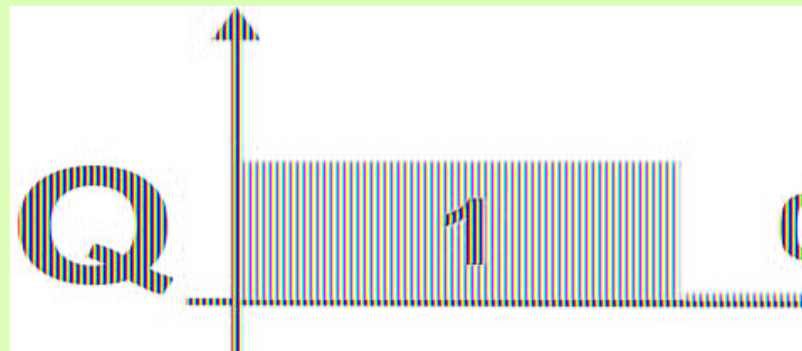
- Elemento básico de memoria.
- Cerrojos o candados.
- Multivibradores biestables o binarios.



Flip Flops

Un Flip Flop es un circuito electrónico digital, llamado también multivibrador biestable, que tiene dos estados estables (0, 1)



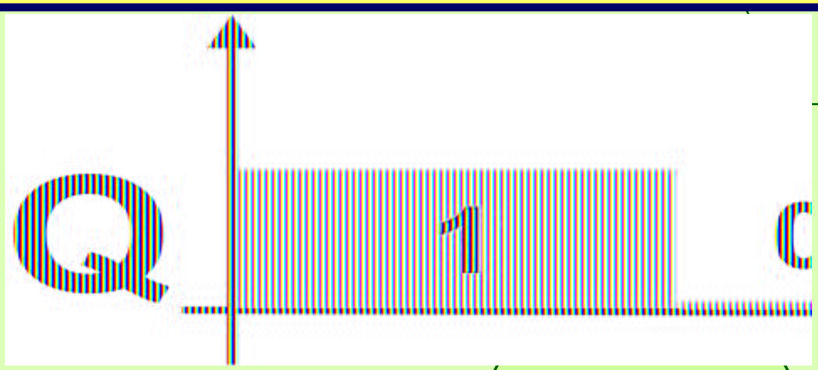


bi-. (Del lat. *bi-*, por *bis*). **.** elem. compos. Significa 'dos' o 'dos veces'

Estable. (Del lat. *stabĭlis*). **.** adj. Que permanece en un lugar durante mucho tiempo.

Flip Flops

El Flip Flop es el elemento de memoria más pequeño que existe y que es capaz de almacenar un número binario de un solo bit.

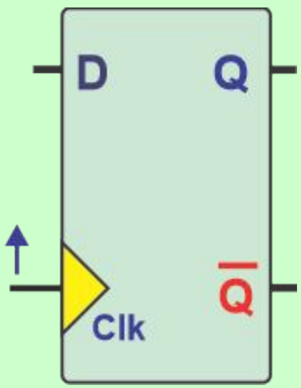
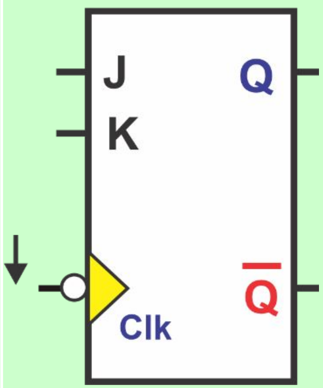
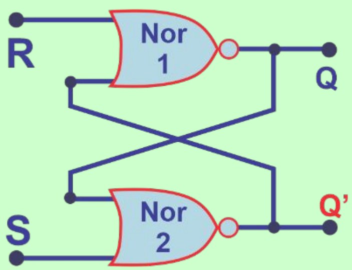
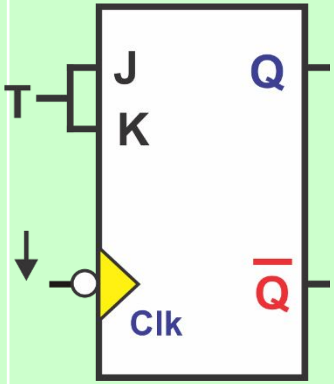
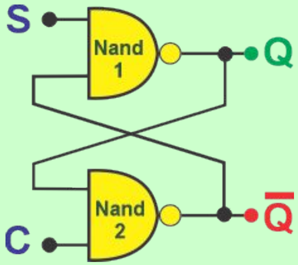


Memoria: Dispositivo físico, generalmente electrónico, en el que se almacenan datos e instrucciones para recuperarlos y utilizarlos posteriormente.

Tipos formales de Flip Flops

Tipo	Nombre	Serie TTL SN 74	
D	**Data o Datos**	**74**, 564, 575, 576, 577, 874, 876	**Flip Flops** Comerciales (estándares)
JK	**Jack Kilby**	**73**, 107, **109**, 112, 276	
SC	**Set Clear**	**279** también llamado **SR**	
RS	**Reset Set**	**Flip Flops** basados en compuertas básicas retroalimentadas o partiendo de FF's comerciales	
T	**Toggle**		
SC	**Set Clear**		

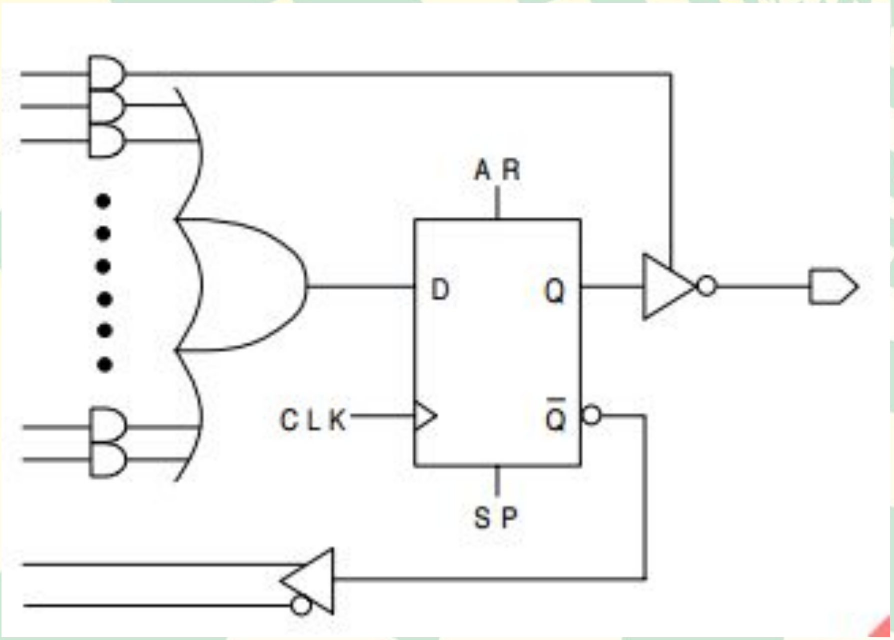
El PLD22V10 tiene 10 FFs tipo D

FF D	FF JK	FF RS	FF T	FF SC
				

Donde hay memoria, hay historia;
donde hay Flip-Flops, hay sistema secuencial

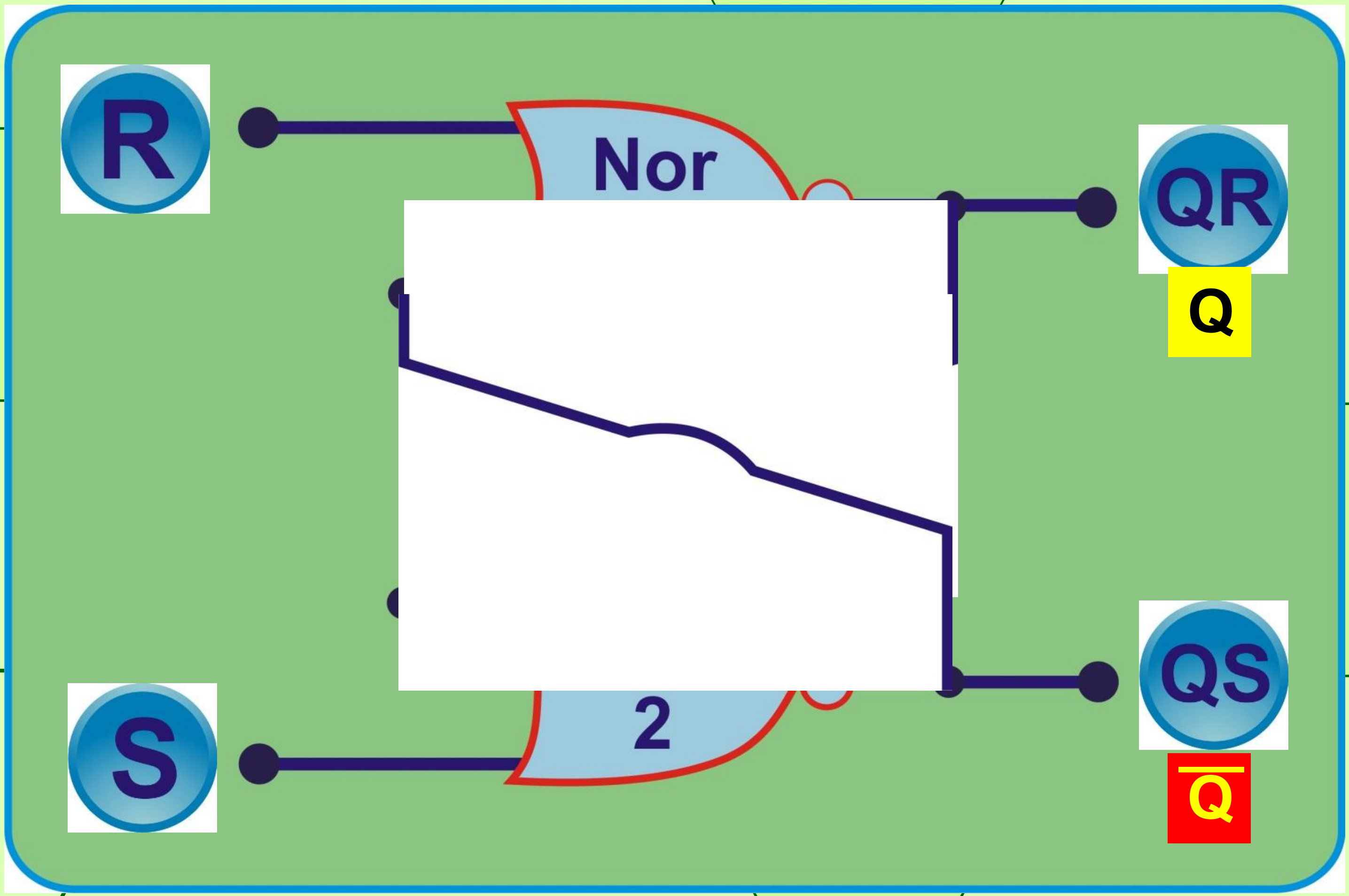
El PLD22V10 tiene 10 FFs tipo D

De las salidas 14 a la 23

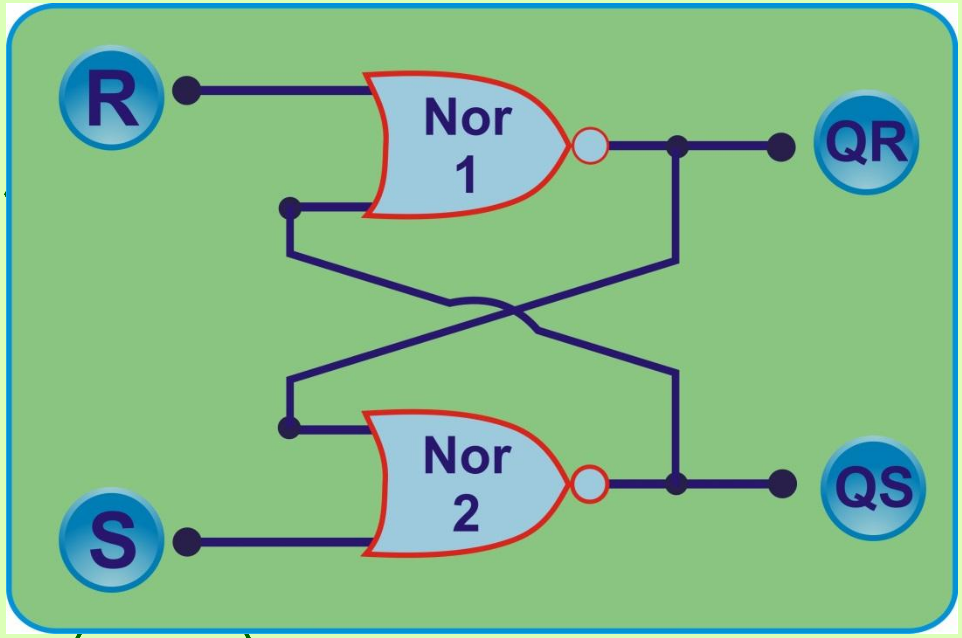


Istype ‘reg’

Flip Flop RS (Reset, Set)



Flip Flop RS (Reset, Set)



$QR = (R+QS)'$

$QS = (S+QR)'$

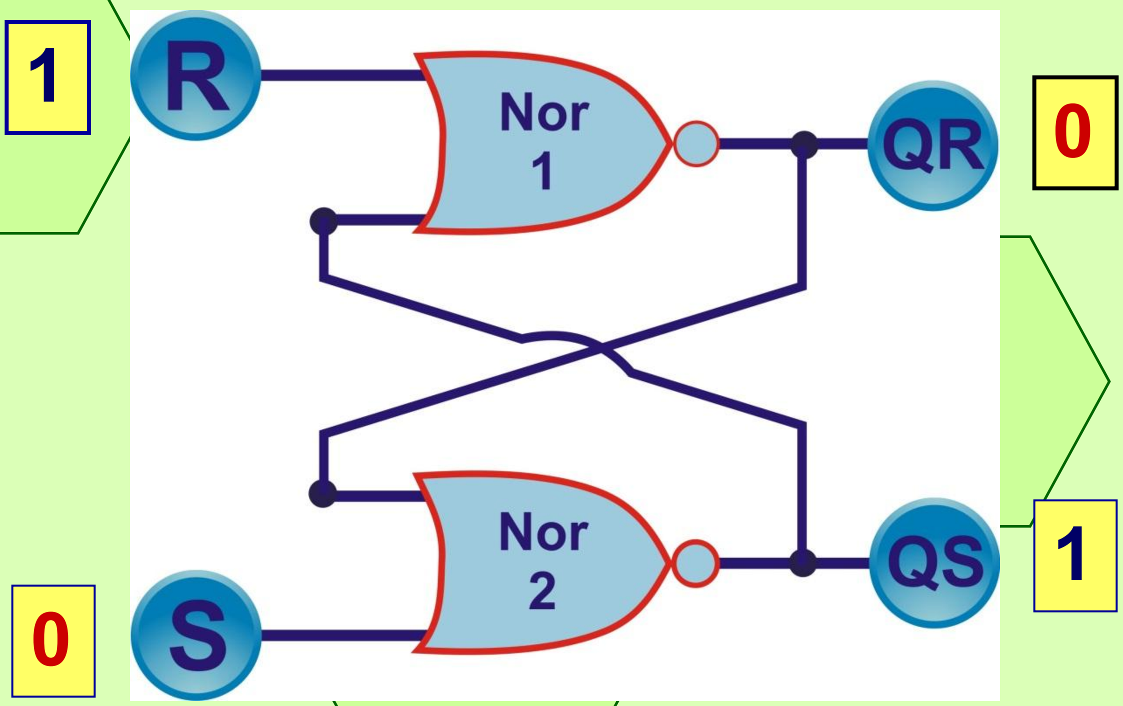
$QR = QS'$

Flip Flop RS (Reset, Set)

Función Reset

Tabla Característica

R	S	QR	QS
1	0	0	1
0	0		
0	1		
0	0		



Flip Flop RS (Reset, Set)

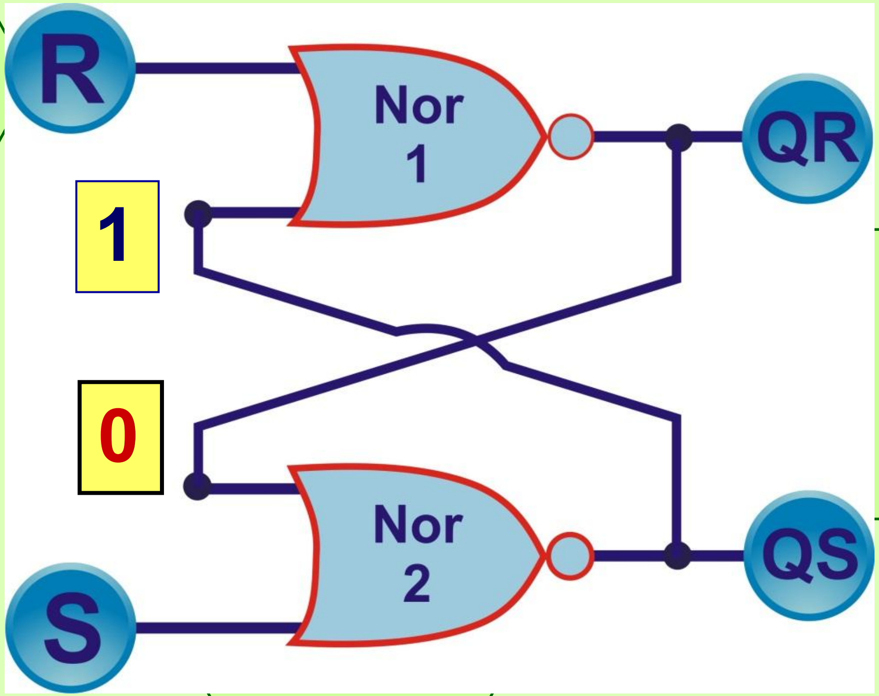
Función Reset

Tabla Característica

R	S	QR	QS
1	0	0	1
0	0		
0	1		
0	0		

1

0



0

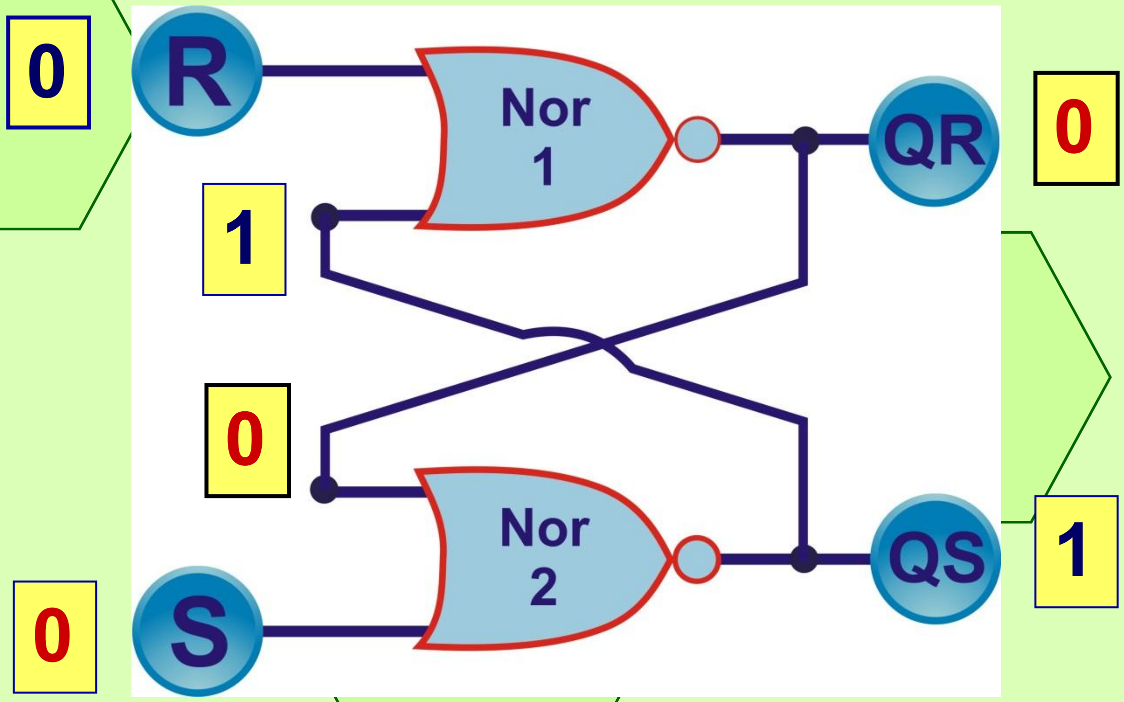
1

Flip Flop RS (Reset, Set)

Función Reset

Tabla Característica

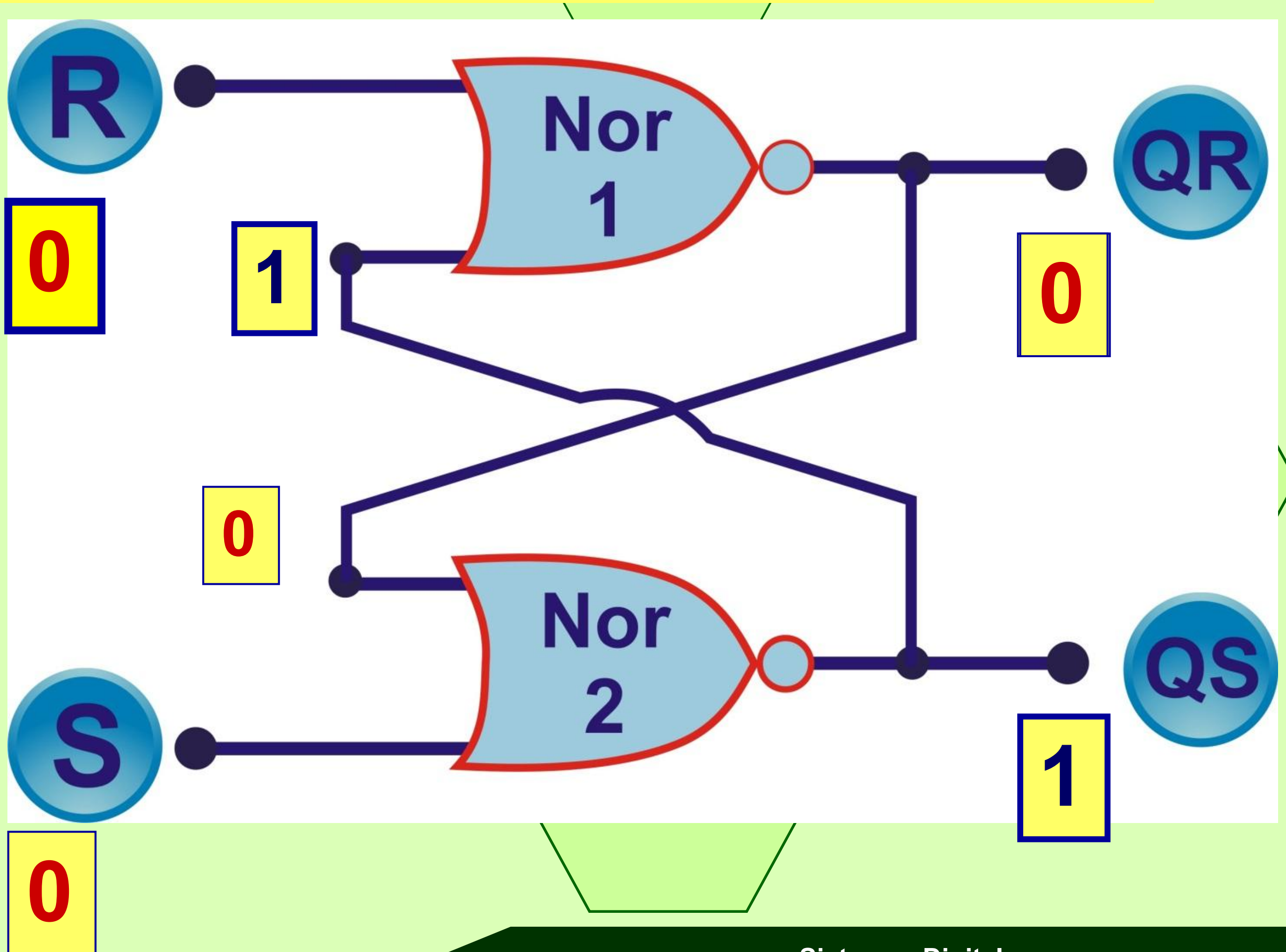
R	S	QR	QS
1	0	0	1
0	0		
0	1		
0	0		



Flip Flop RS (Reset, Set)

Que pasará con los valores de salida si cambiamos el valor de R=0

R	S	QR	QS
1	0	0	1
0	0	0	1
0	1		
0	0		

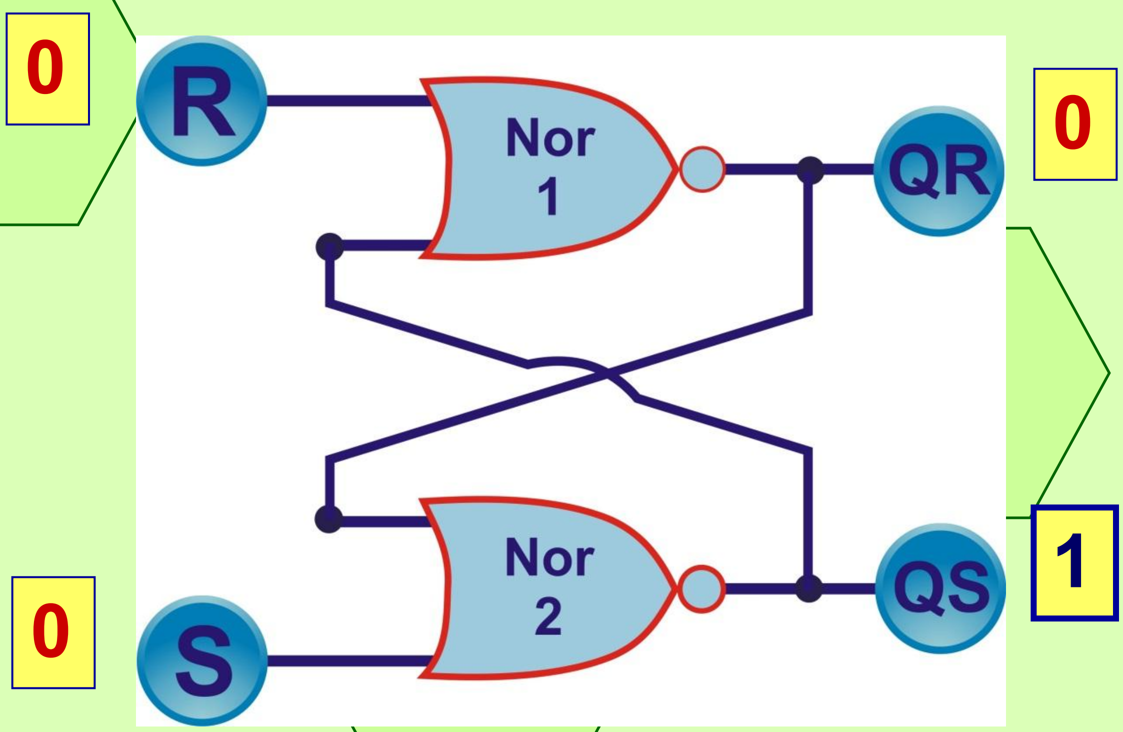


Flip Flop RS (Reset, Set)

Función Memoria del Reset

Tabla Característica

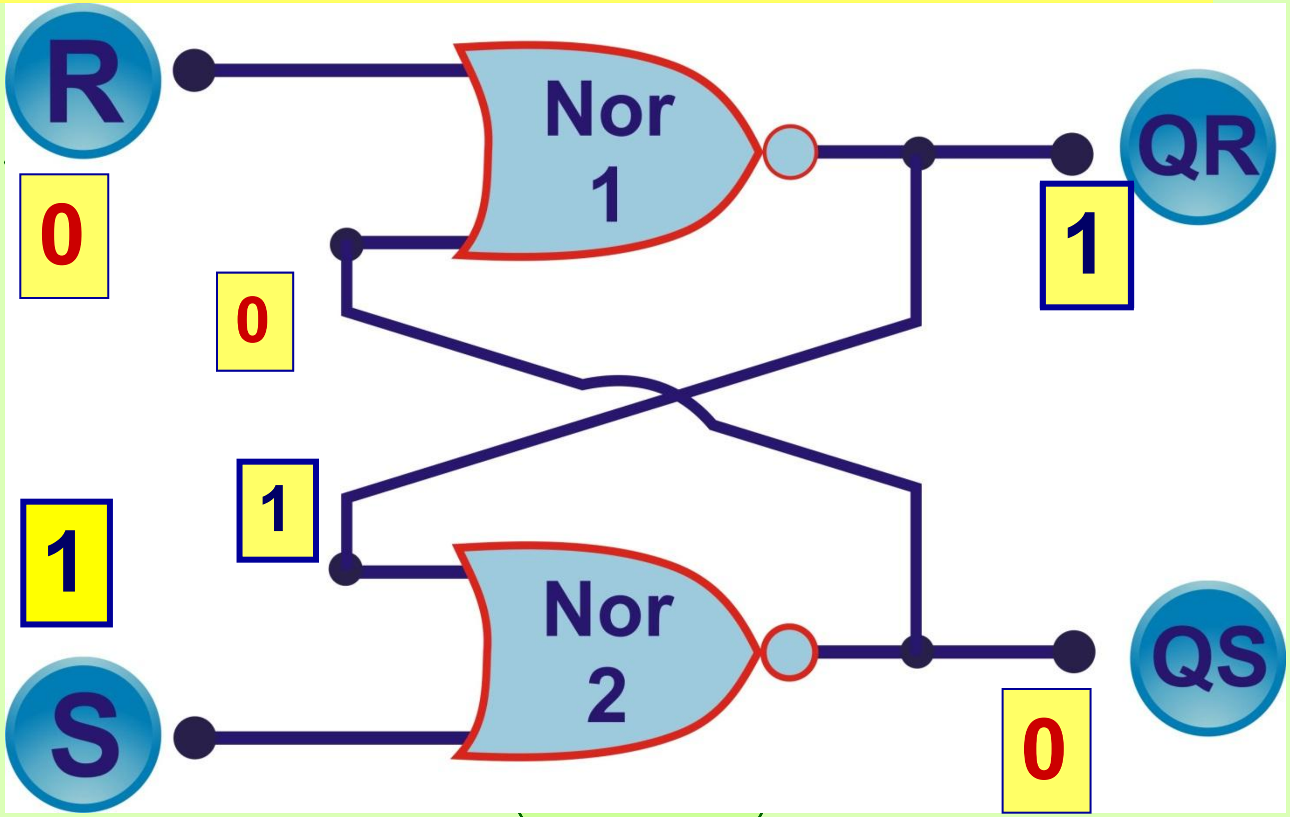
R	S	QR	QS
1	0	0	1
0	0	0	1
0	1		
0	0		



Flip Flop RS (Reset, Set)

Que pasará con los valores de salida si cambiamos S=1

R	S	QR	QS
1	0	0	1
0	0	0	1
0	1	1	0
0	0		

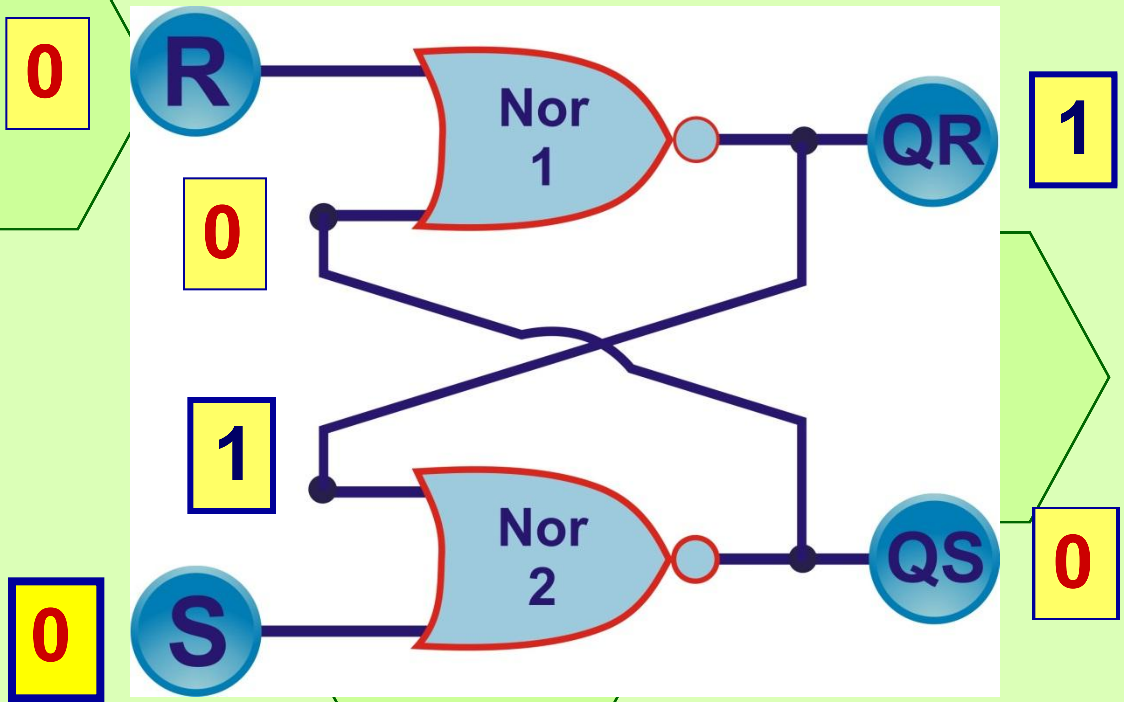


Flip Flop RS (Reset, Set)

Que pasará con los valores de salida si cambiamos S=0

Tabla Característica

R	S	QR	QS
1	0	0	1
0	0	0	1
0	1	1	0
0	0	1	0

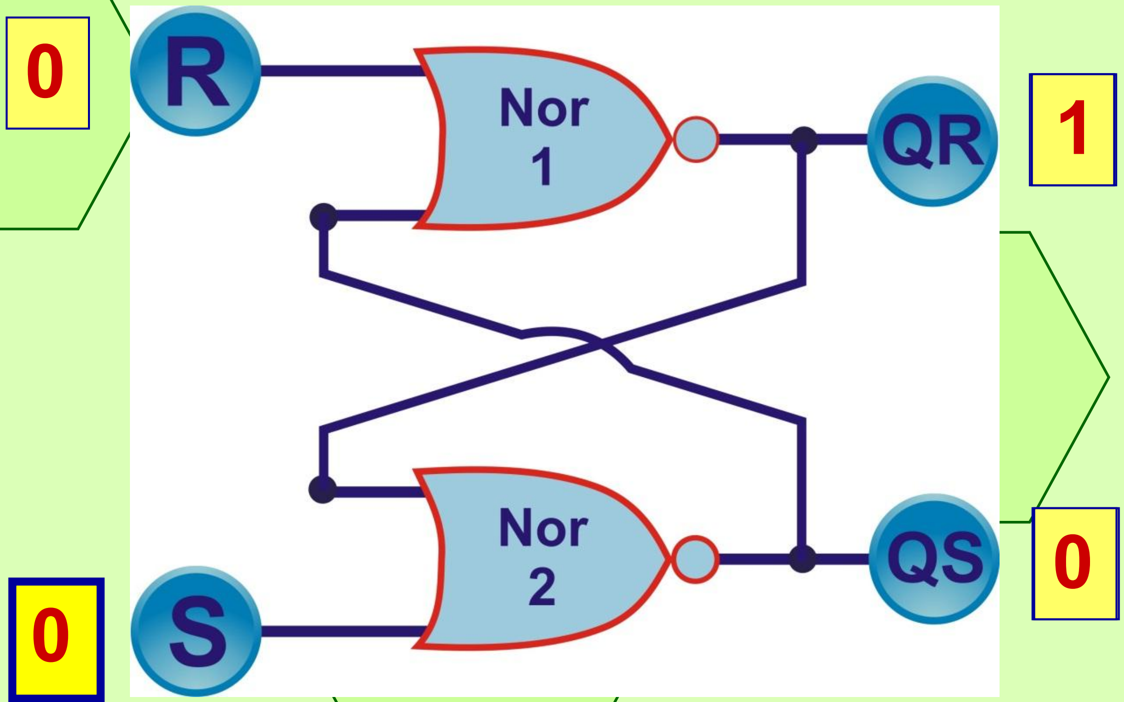


Flip Flop RS (Reset, Set)

Función Memoria del Set

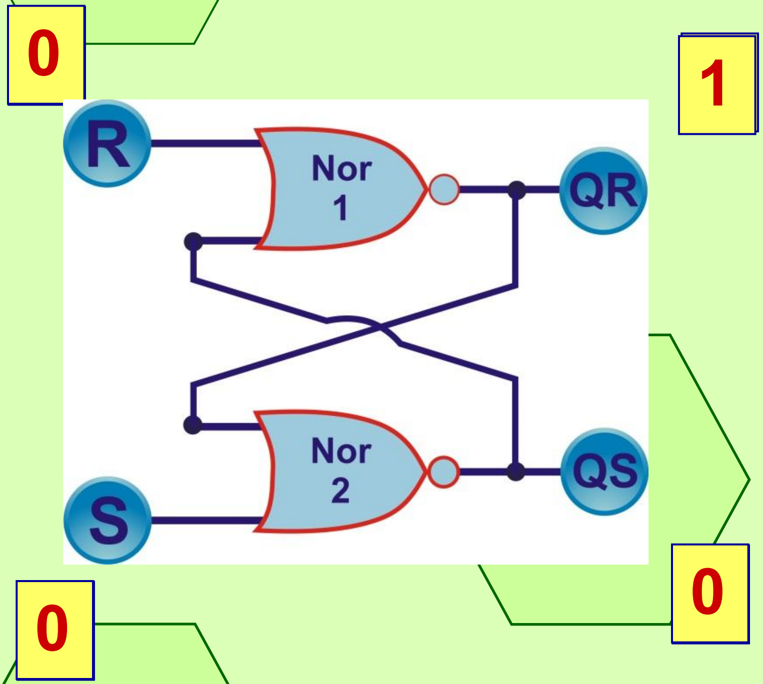
Tabla Característica

R	S	QR	QS
1	0	0	1
0	0	0	1
0	1	1	0
0	0	1	0

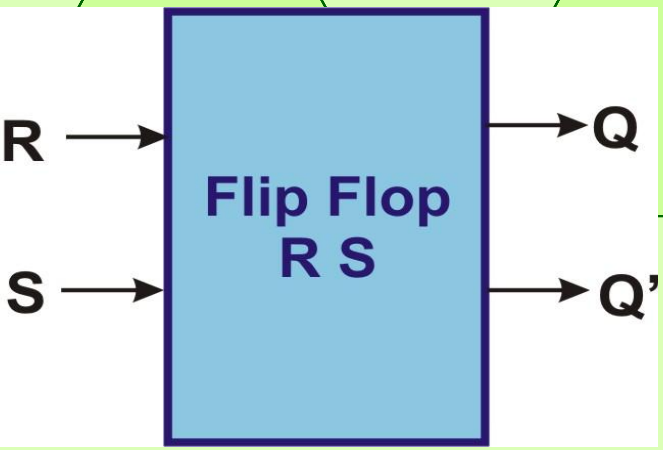


Flip Flop RS (Reset, Set)

Acción	R	S	Q	Q’
Reset	1	0	0	1
Memoria	0	0	0	1
Set	0	1	1	0
Memoria	0	0	1	0



Flip Flop RS (Reset, Set)



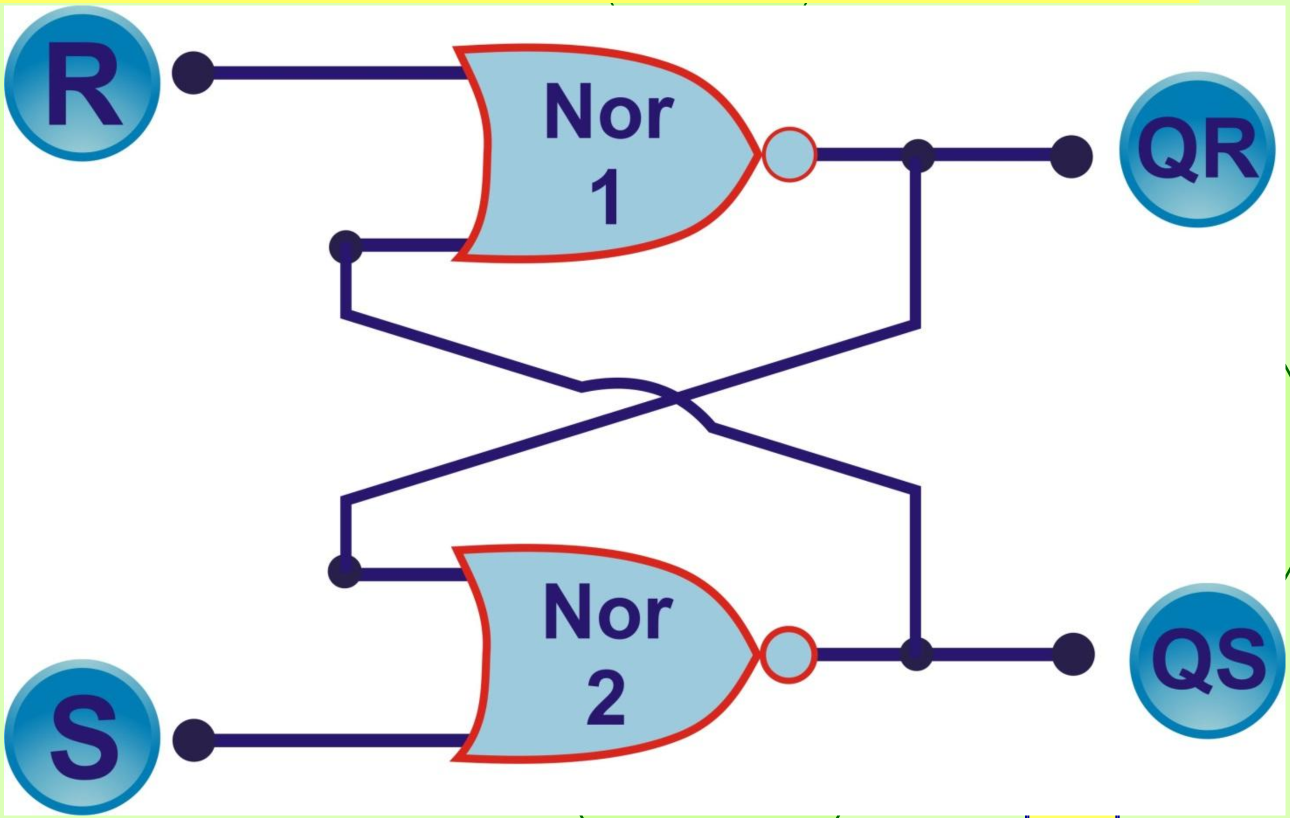
R	S	Qn+1	Q’
0	0	Q	Q’
0	1	1	0
1	0	0	1

Qn+1 = el valor próximo de Q

Flip Flop RS Condición no estable

Qué pasará con los valores de salida si R=1 y S=1

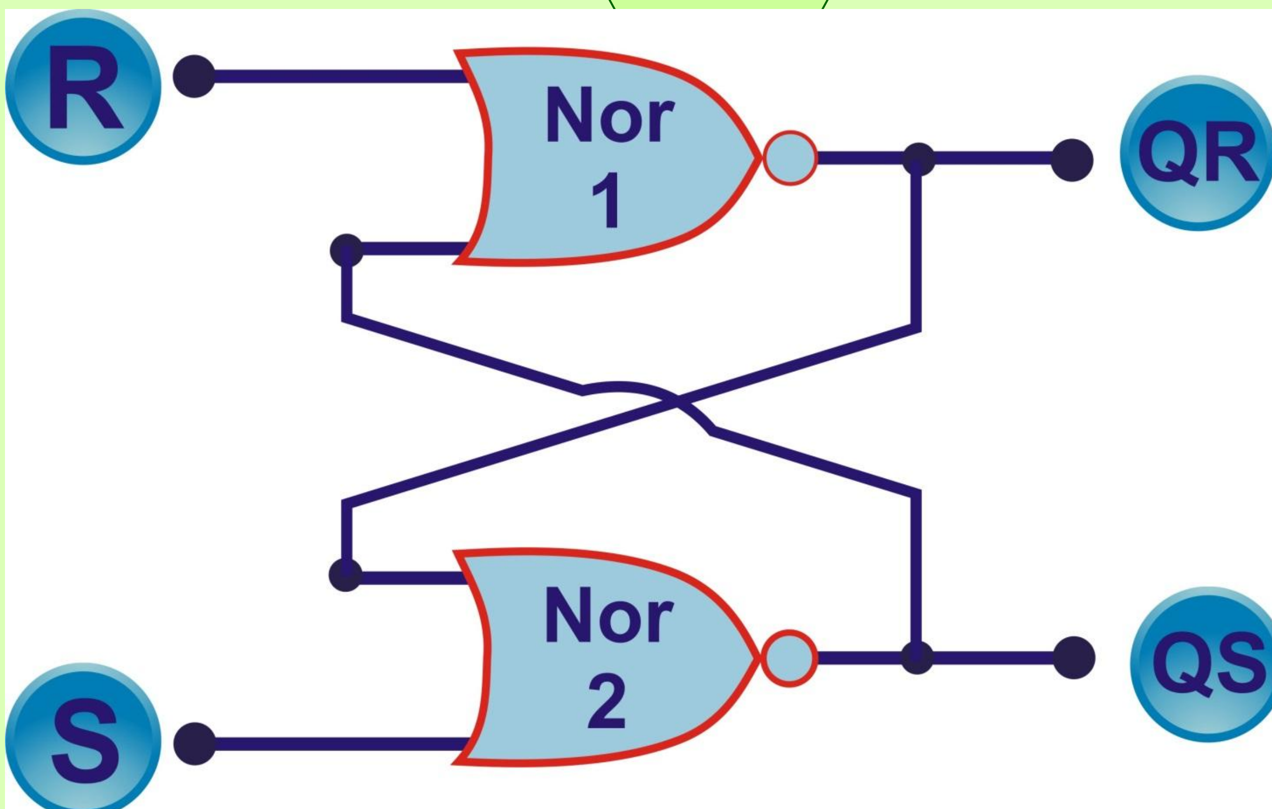
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0



1

Flip Flop RS Condición no estable

R	S	Qn+1	Q’
0	0	Q	Q’
0	1	1	0
1	0	0	1
1	1	0	0

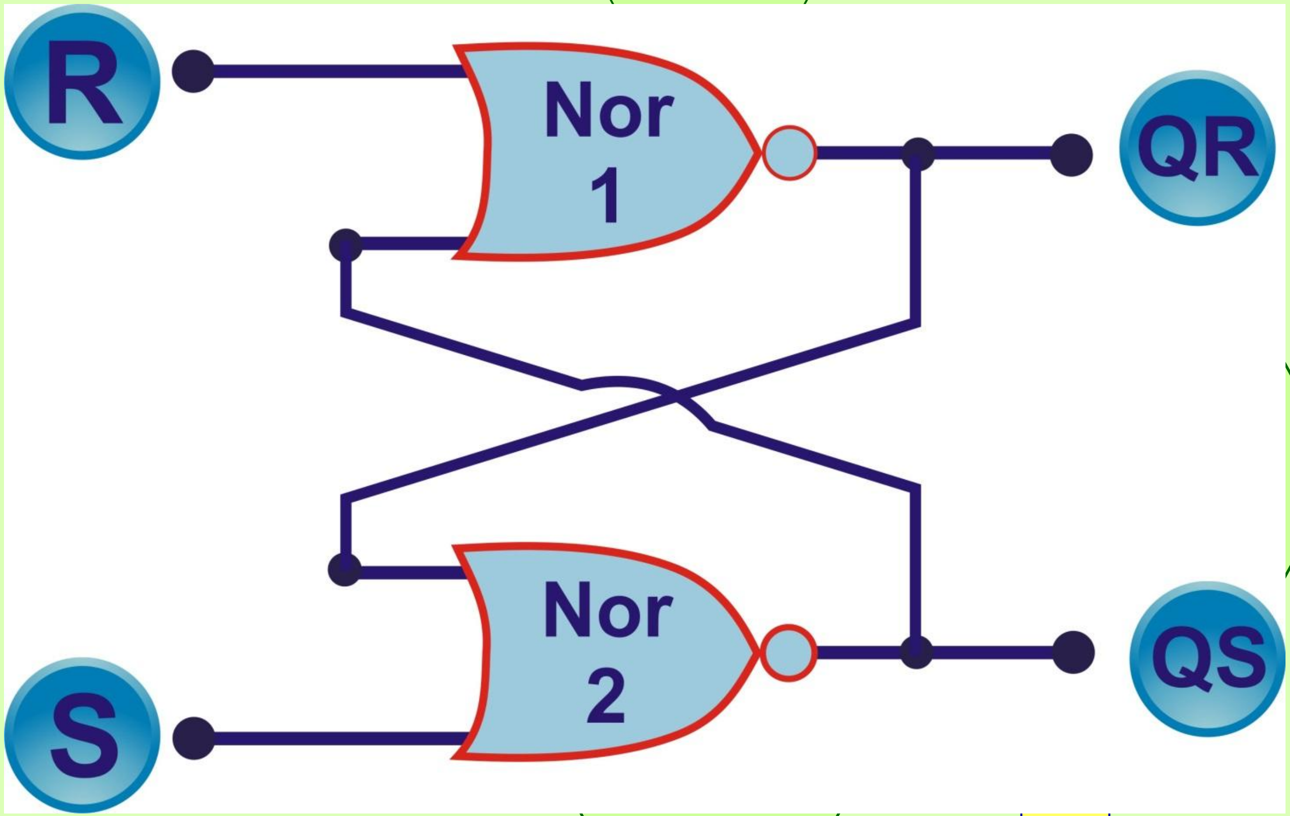


1

Flip Flop RS Condición no estable

Si después de haber dado la combinación R=1 y S=1 tratamos de memorizar R=0 y S=0

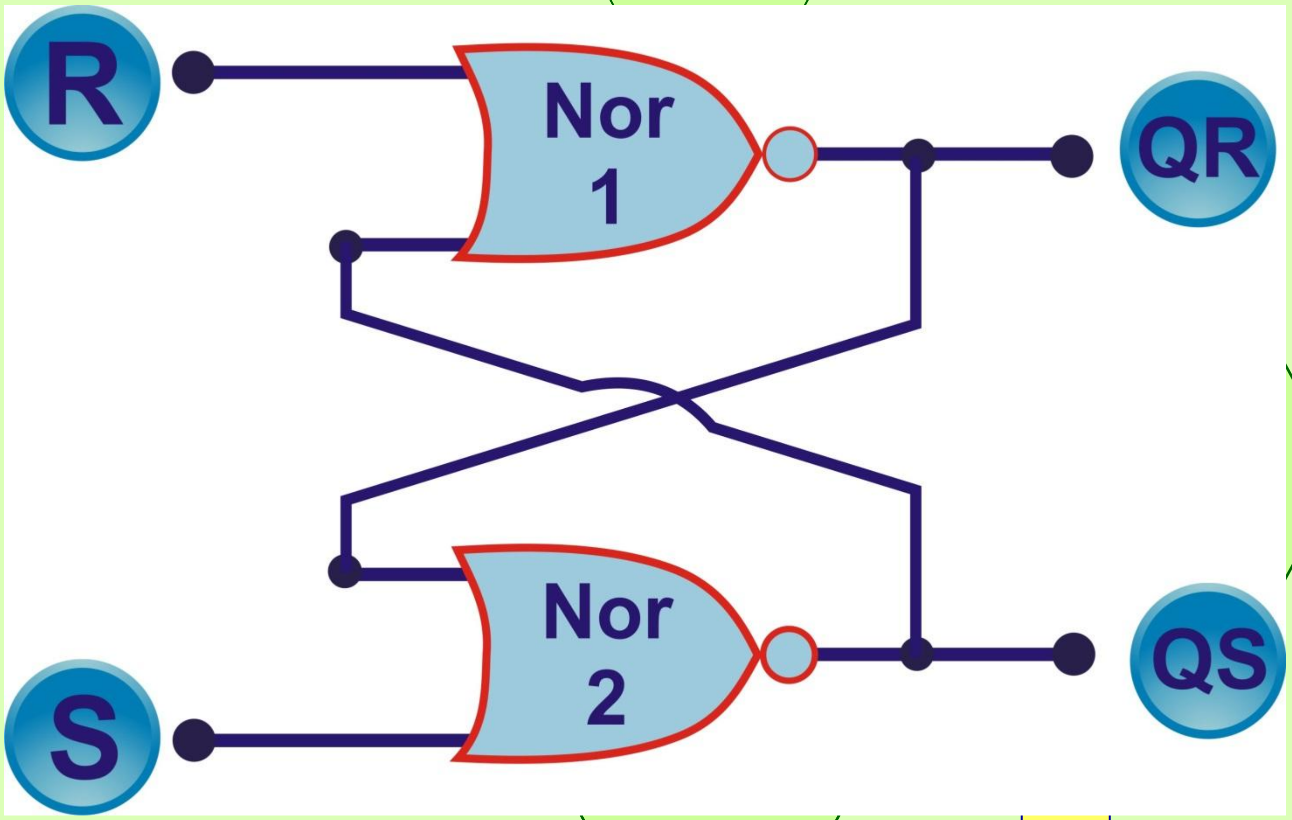
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0



0

Flip Flop RS
Reset Set

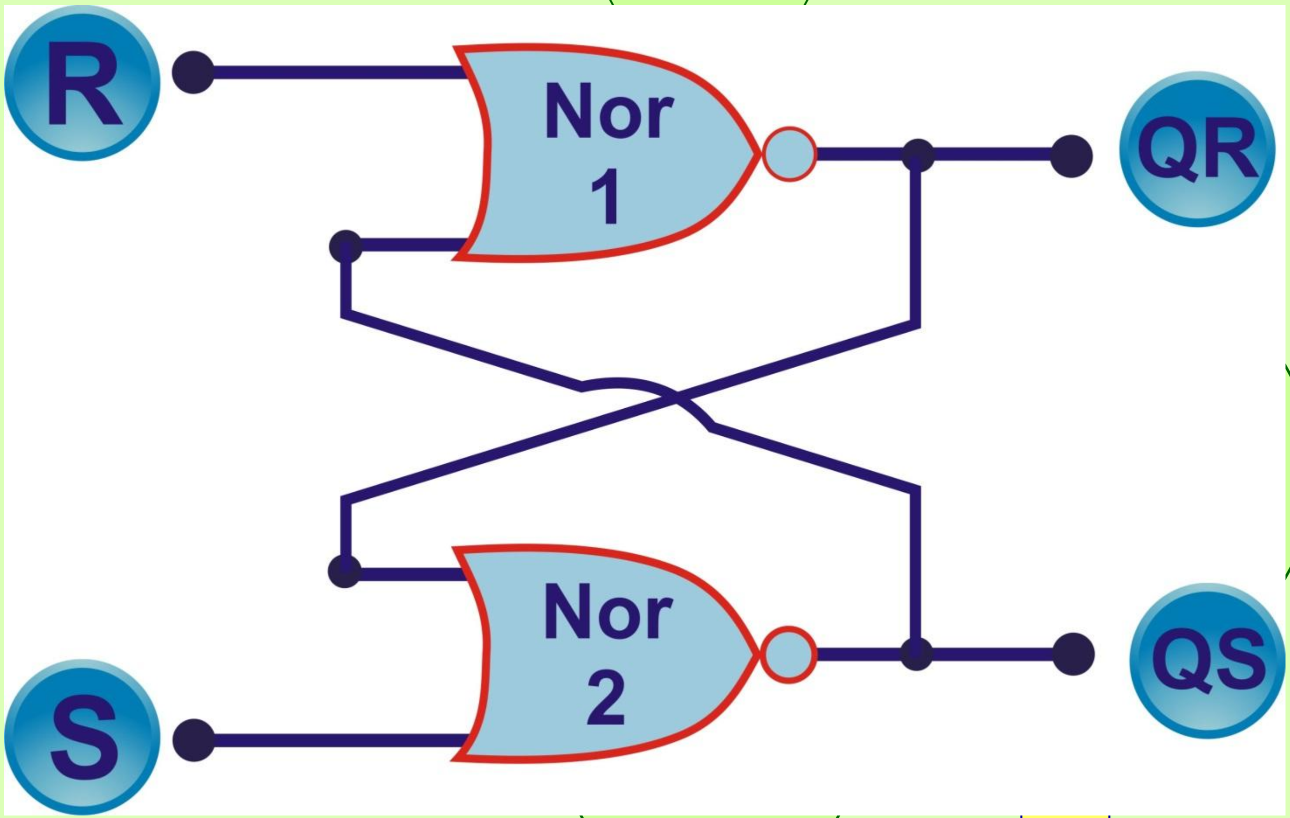
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0



0

Flip Flop RS
Reset Set

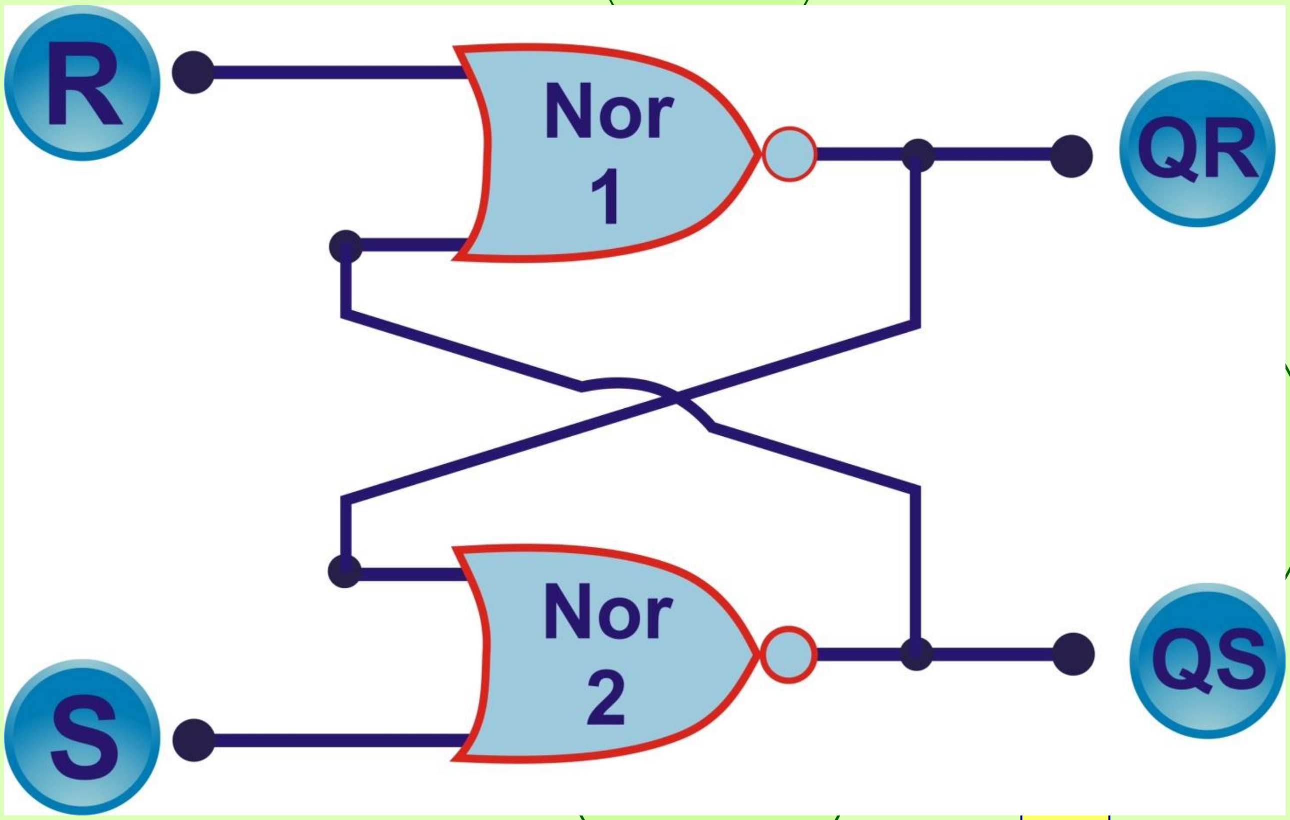
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0



0

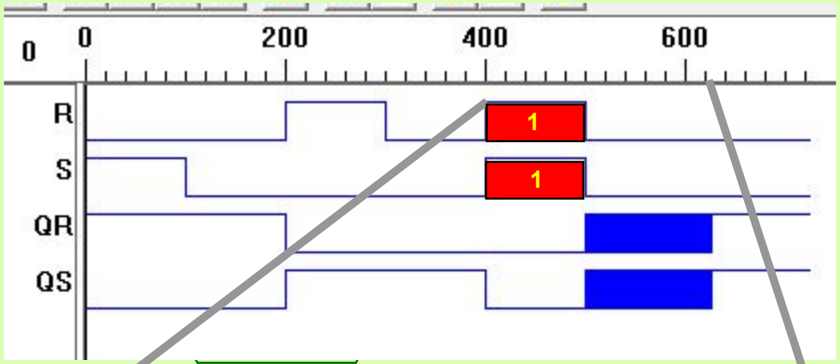
Flip Flop RS
Reset Set

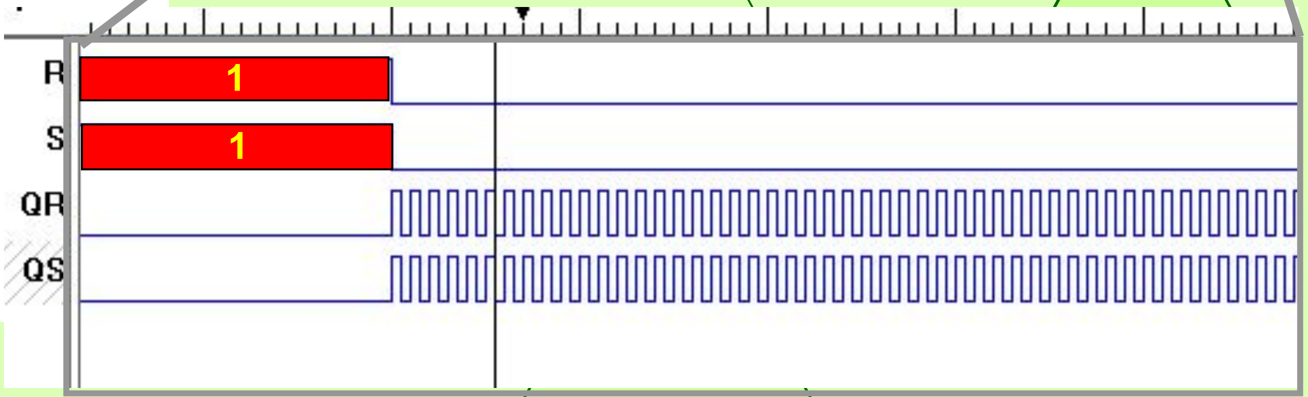
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0



0

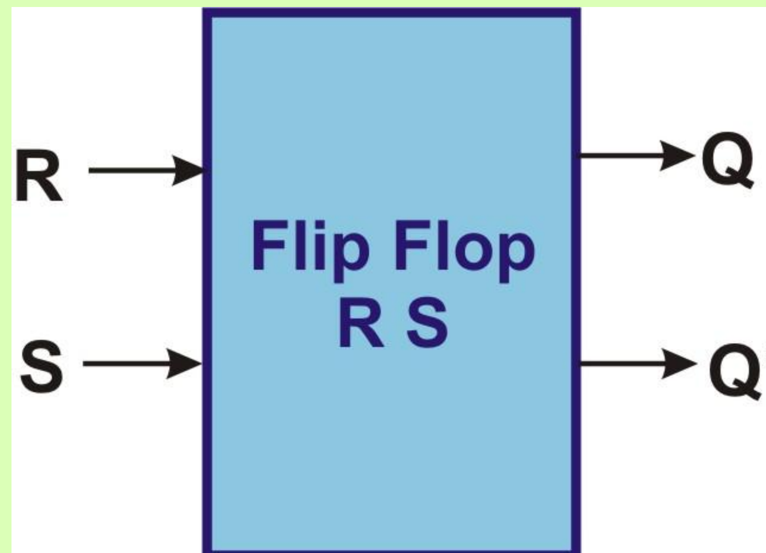
```
MODULE frsa
"Entradas
R,S pin 1,2;
"Salidas
QR,QS pin 19,18 istype 'com';
equations
QR=!(R#QS);
QS=!(S#QR);
Test_vectors
([R,S]->[QR,QS])
[1,0]->[.x.,.x.];
[0,0]->[.x.,.x.];
[1,1]->[.x.,.x.];
[0,0]->[.x.,.x.];
END
```

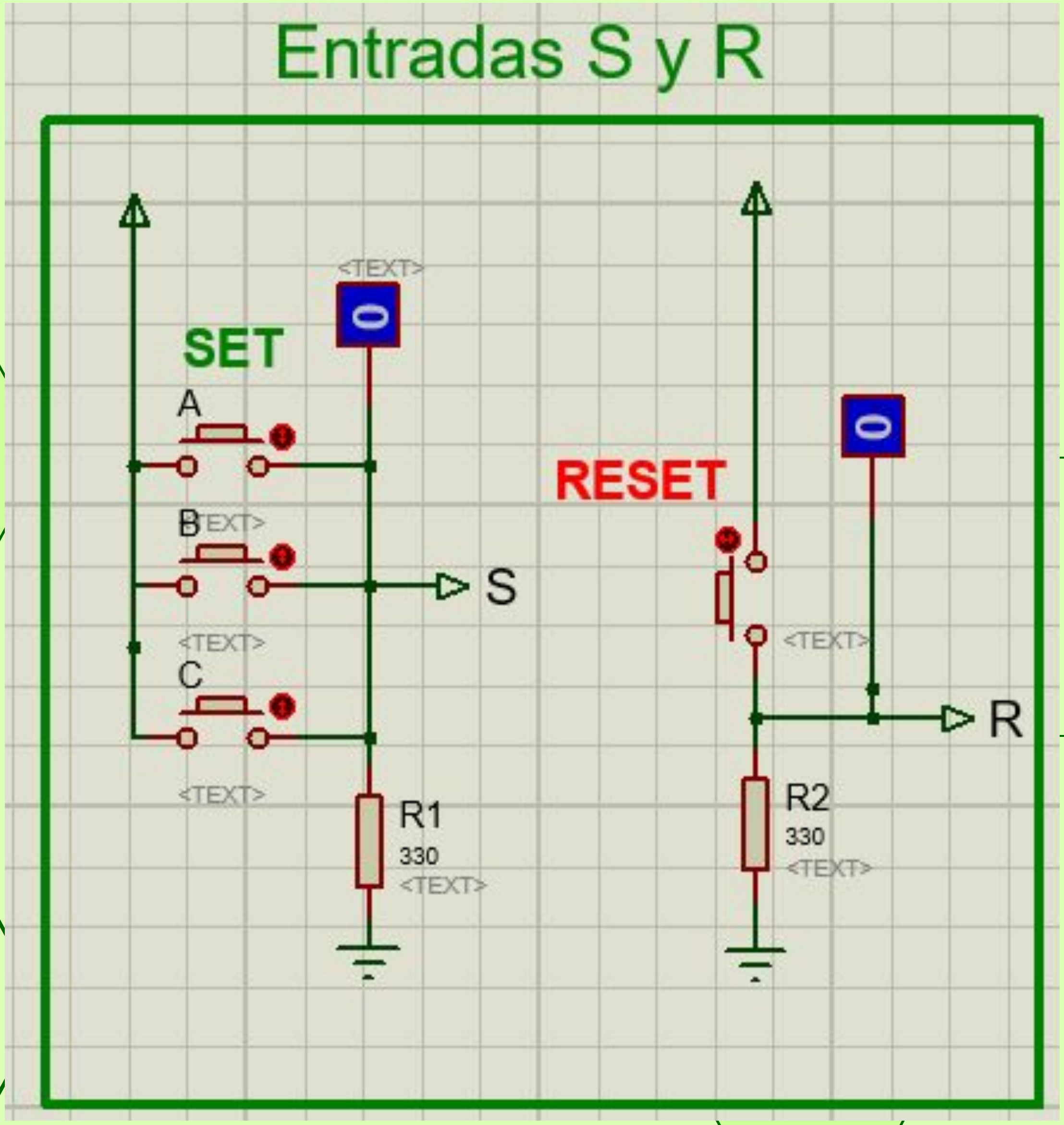


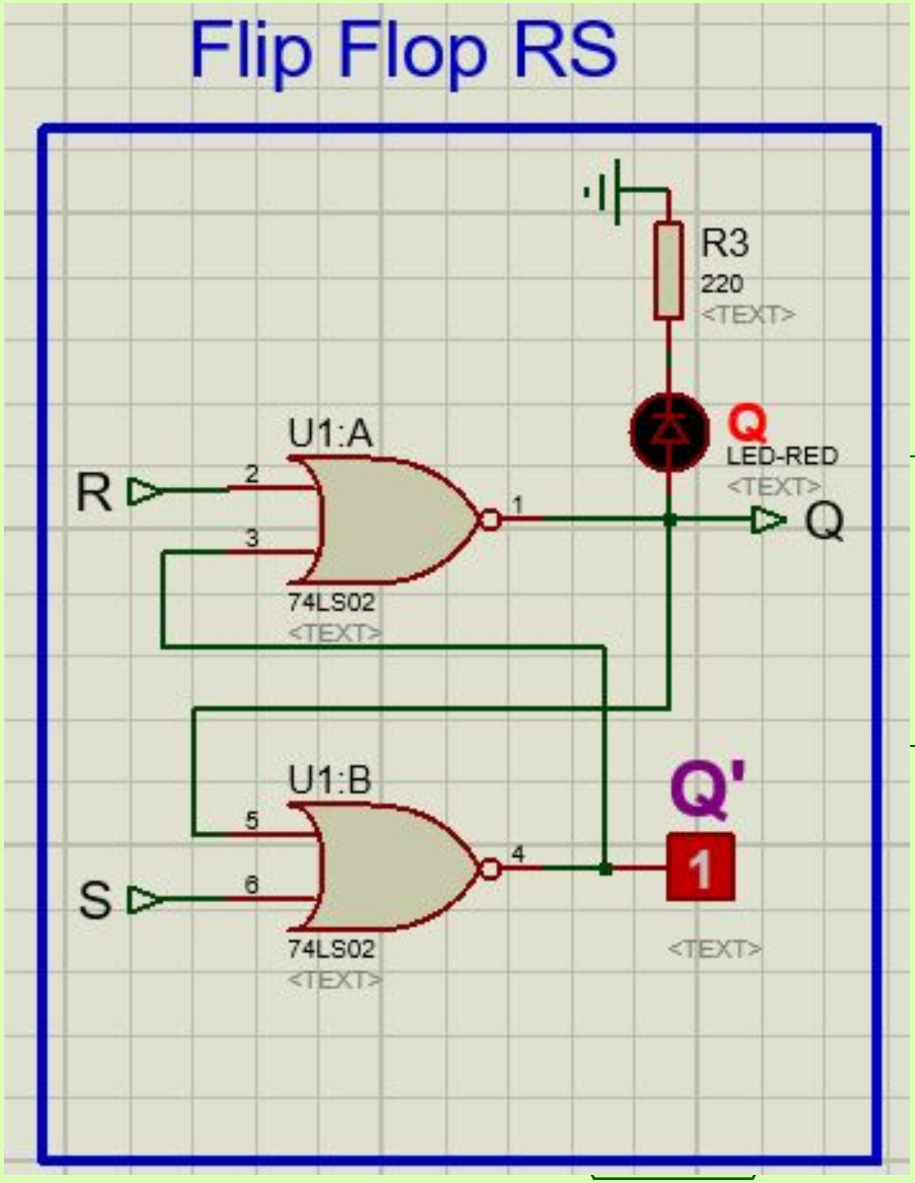


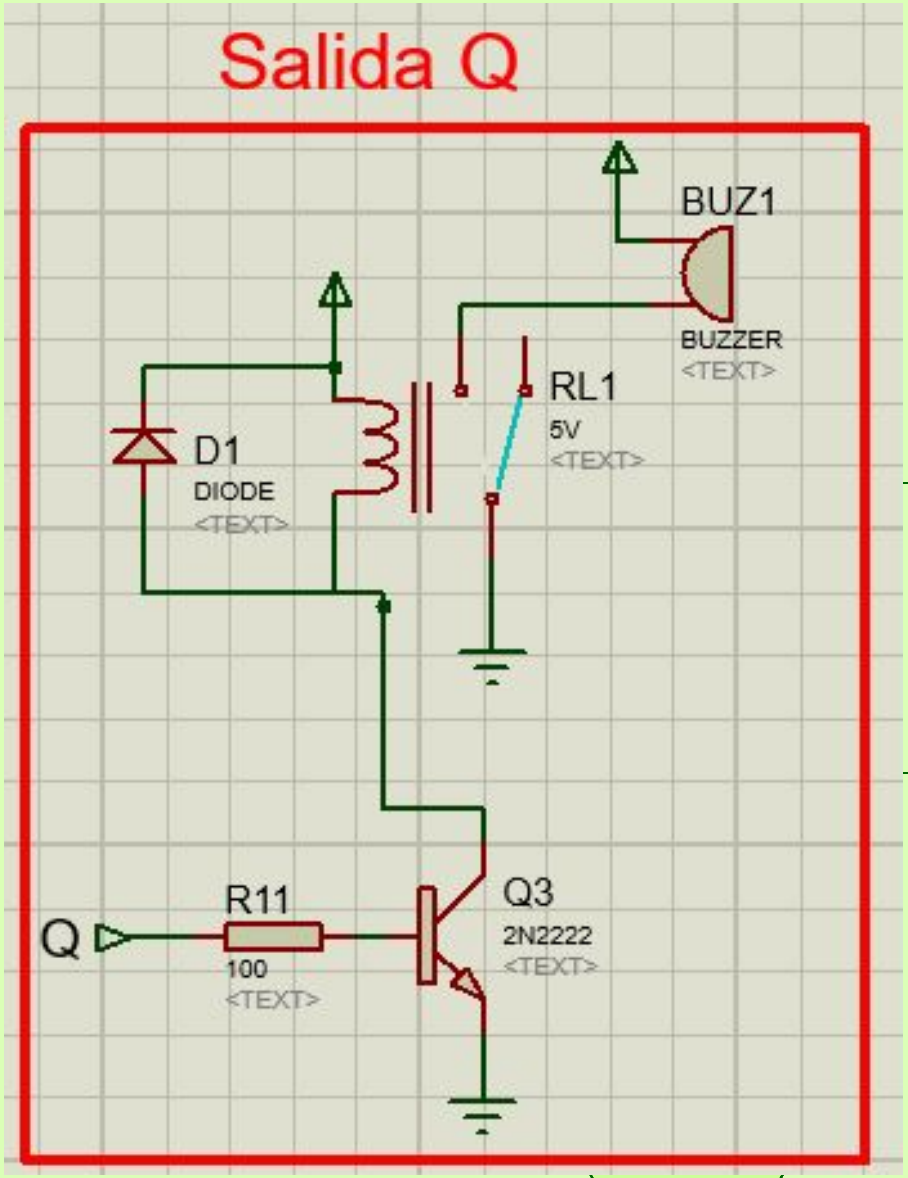
Flip Flop RS
Tabla Característica

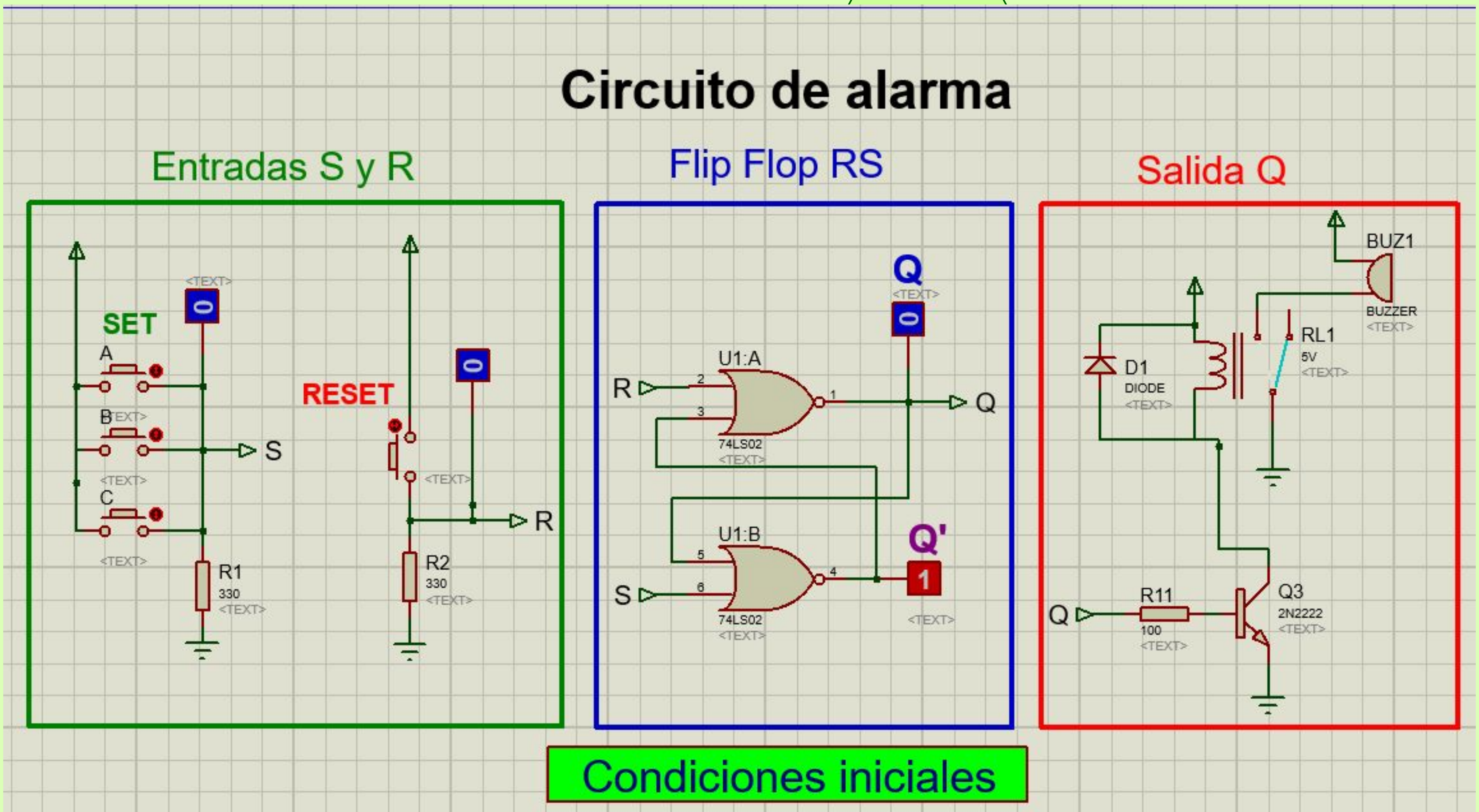
R	S	Qn+1	Q’
0	0	Q	Q’
0	1	1	0
1	0	0	1
1	1	0	0

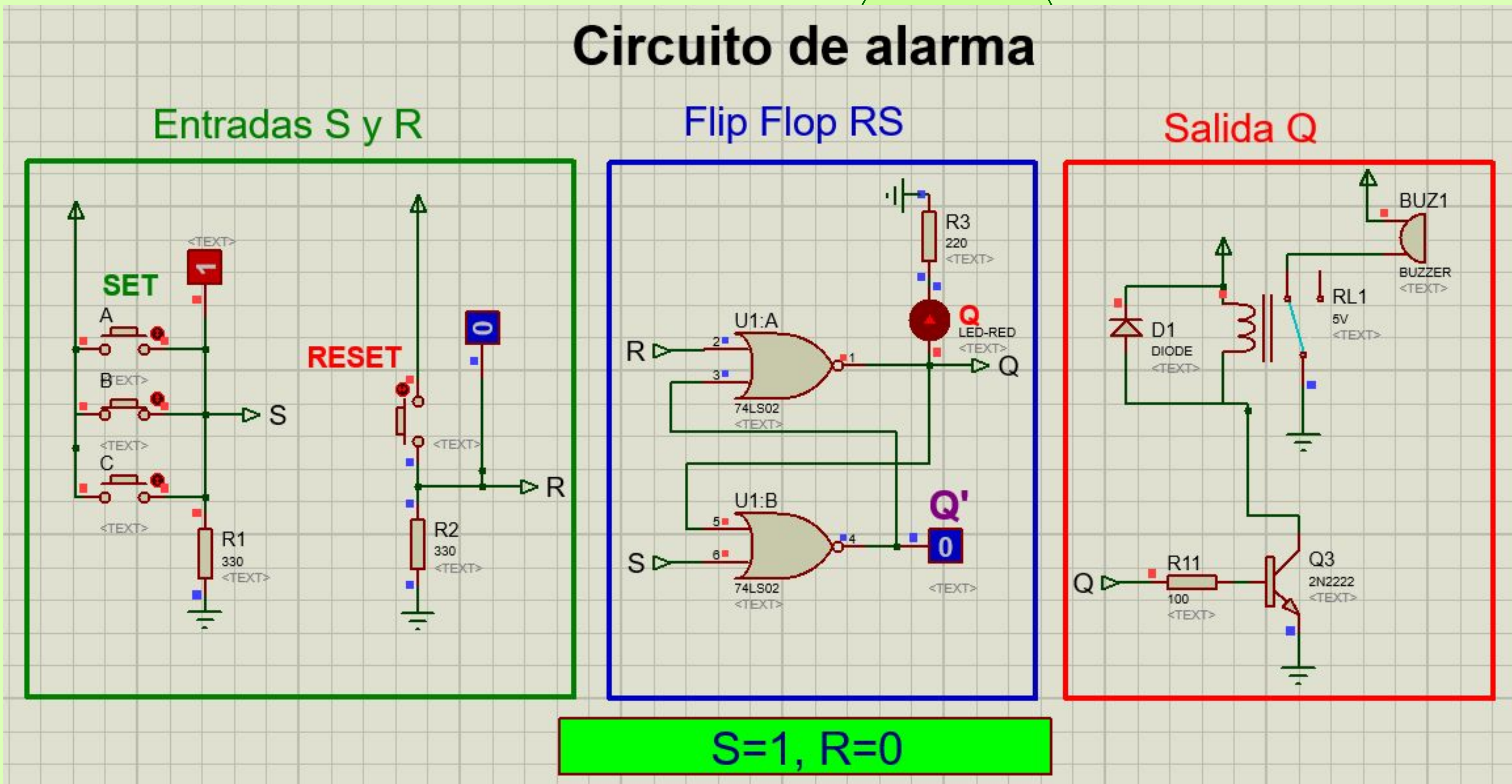



Entradas S y R
SET
A
B
C
<TEXT>
0
S
R1
330
RESET
0
R
R2
330

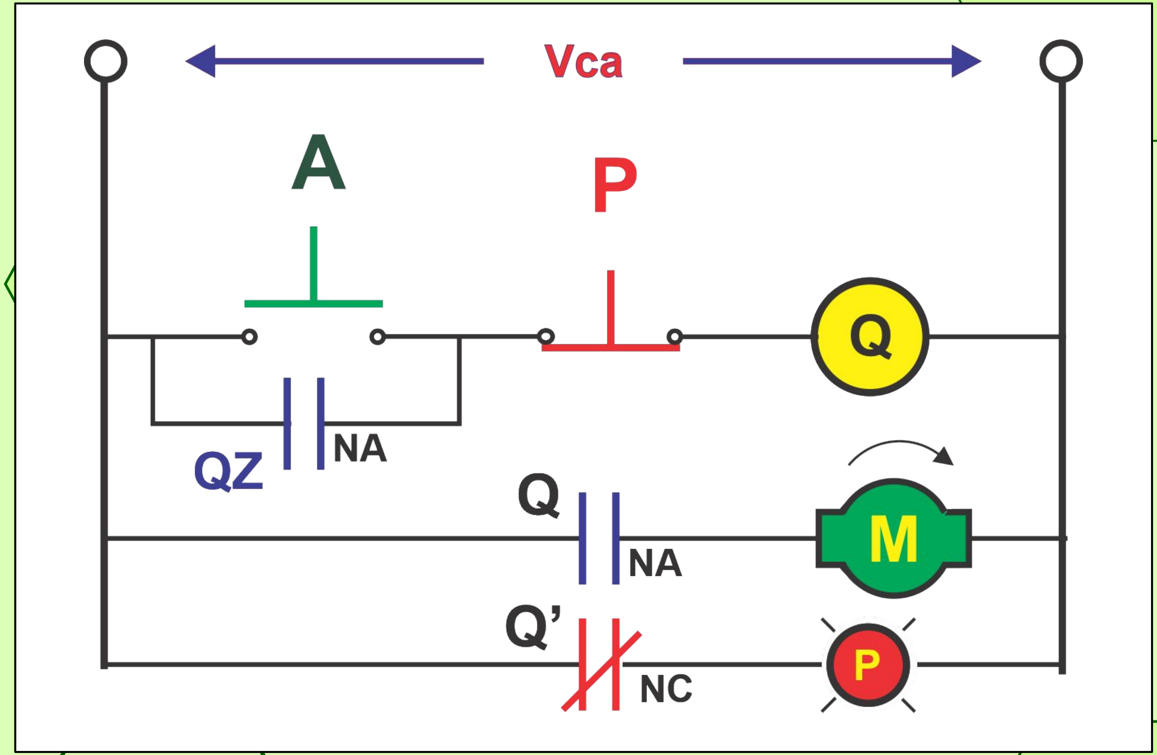

Flip Flop RS
R3
220
<TEXT>
Q
LED-RED
<TEXT>
U1:A
2
3
1
R
Q
74LS02
<TEXT>
U1:B
5
6
4
S
Q'
1
74LS02
<TEXT>
<TEXT>

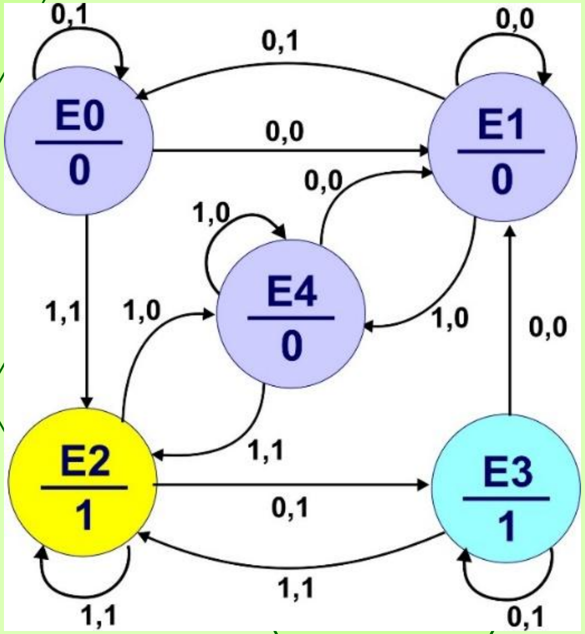

Salida Q
BUZ1
BUZZER
<TEXT>
RL1
5V
<TEXT>
D1
DIODE
<TEXT>
Q
R11
100
<TEXT>
Q3
2N2222
<TEXT>


Circuito de alarma
Entradas S y R
Flip Flop RS
Salida Q
SET
A
B
C
S
RESET
R
R1
330
R2
330
U1:A
74LS02
U1:B
74LS02
Q
Q'
0
1
D1
DIODE
RL1
5V
BUZ1
BUZZER
R11
100
Q3
2N2222
Condiciones iniciales


Circuito de alarma
Entradas S y R
Flip Flop RS
Salida Q
SET
A
B
C
S
RESET
R
R1
330
R2
330
R3
220
U1:A
U1:B
74LS02
Q
LED-RED
Q'
0
1
D1
DIODE
RL1
5V
BUZ1
BUZZER
R11
100
Q3
2N2222
S=1, R=0

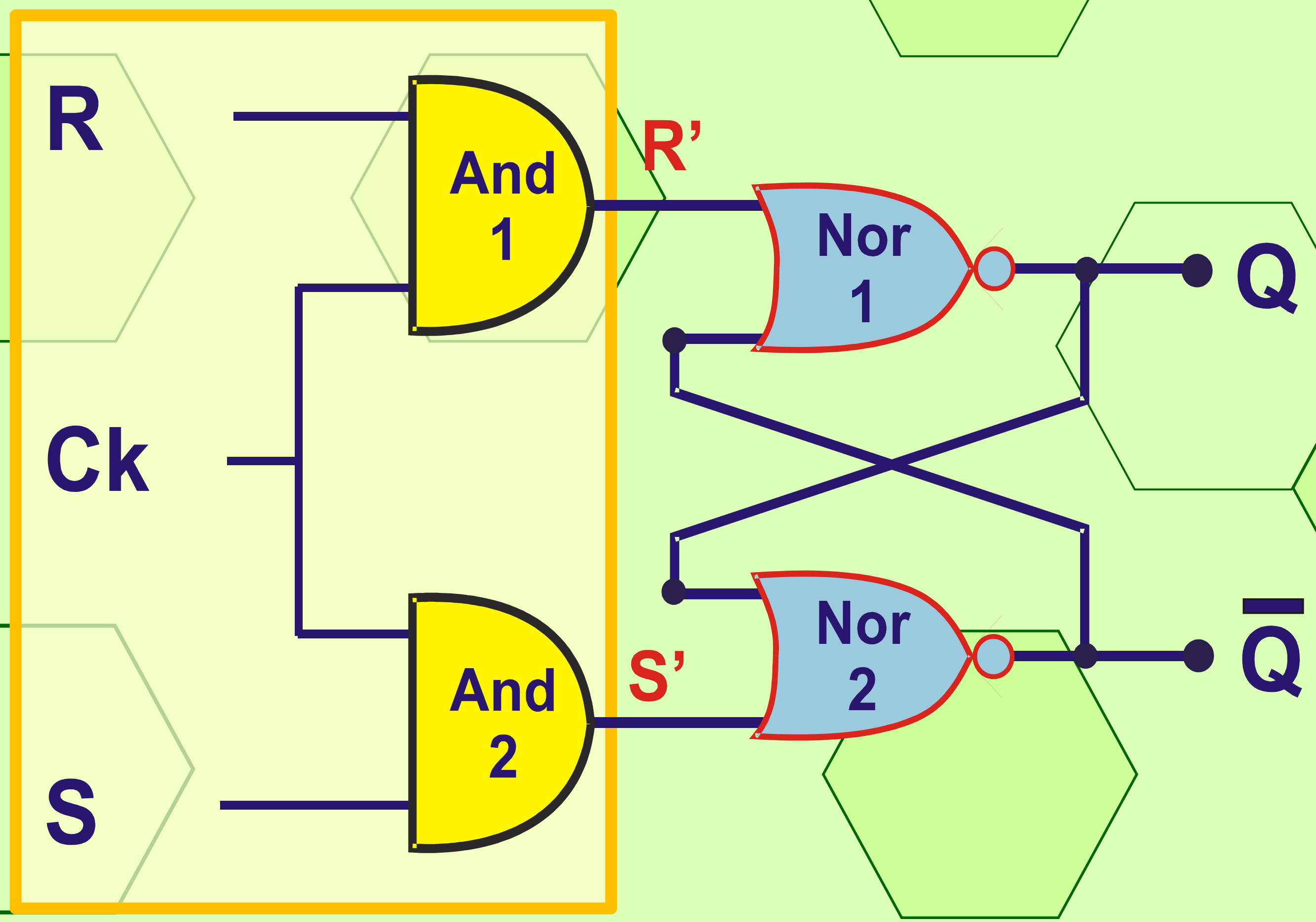
Circuito de Arranque y Paro de un motor



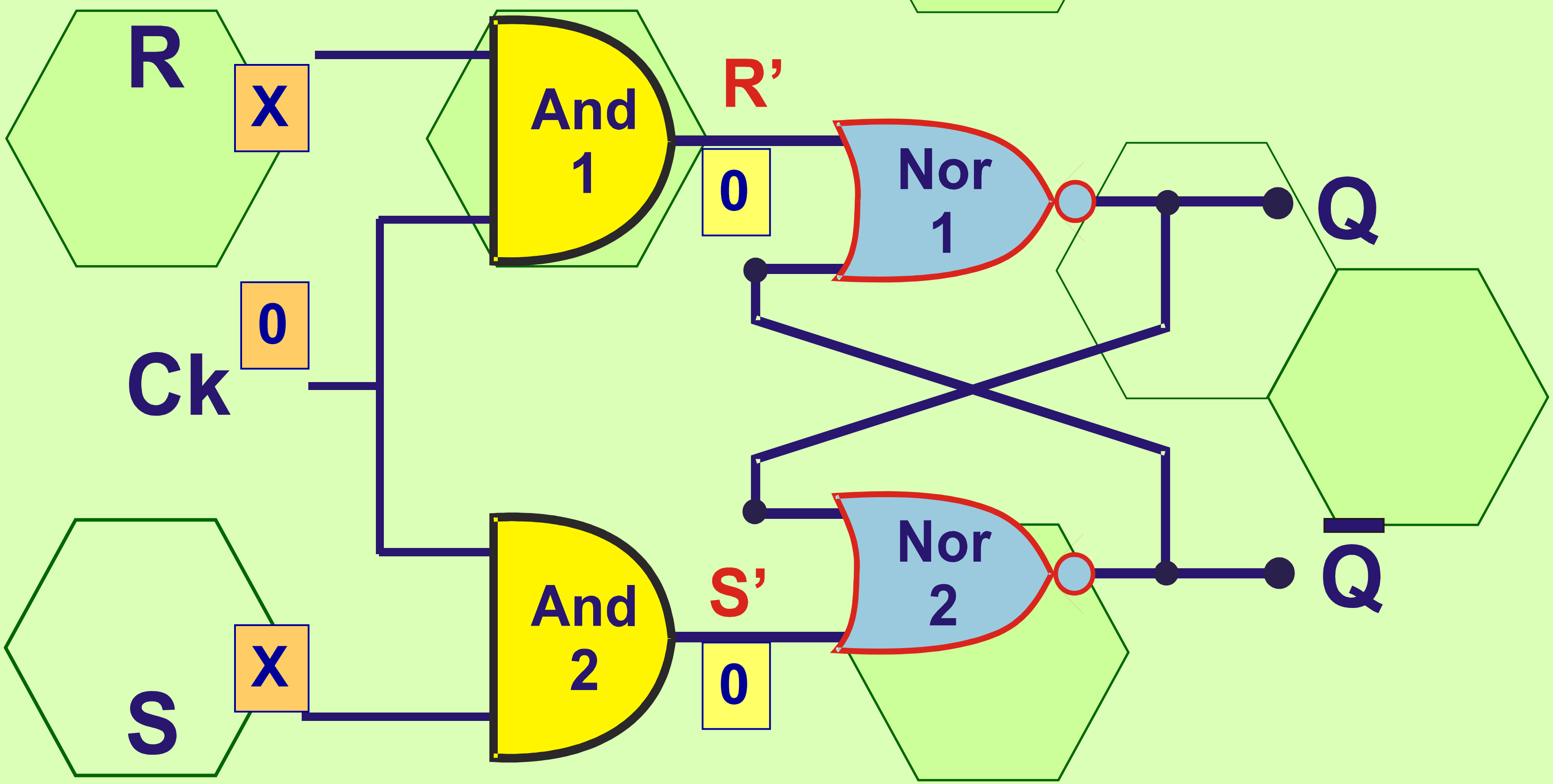


$$Q = P'(A+Q)$$

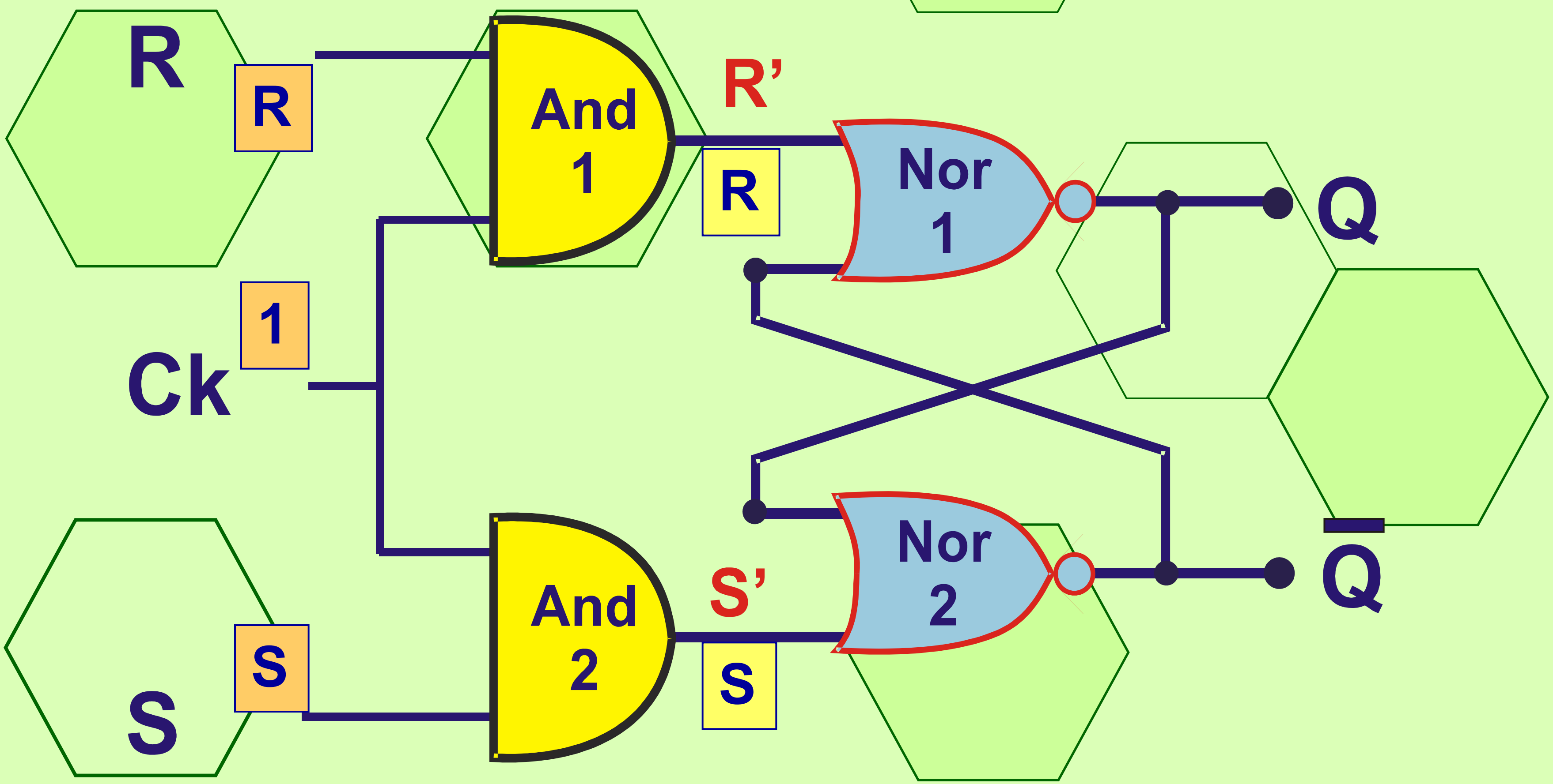
Flip Flop RS
Señal de sincronía Ck



Flip Flop RS
Señal de sincronía Ck

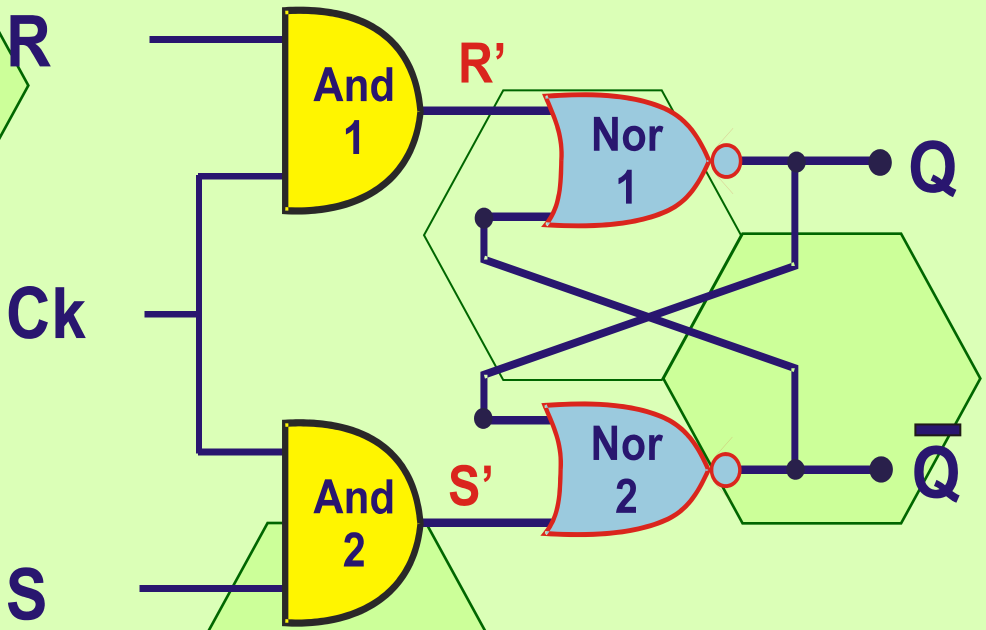


Flip Flop RS
Señal de sincronía Ck

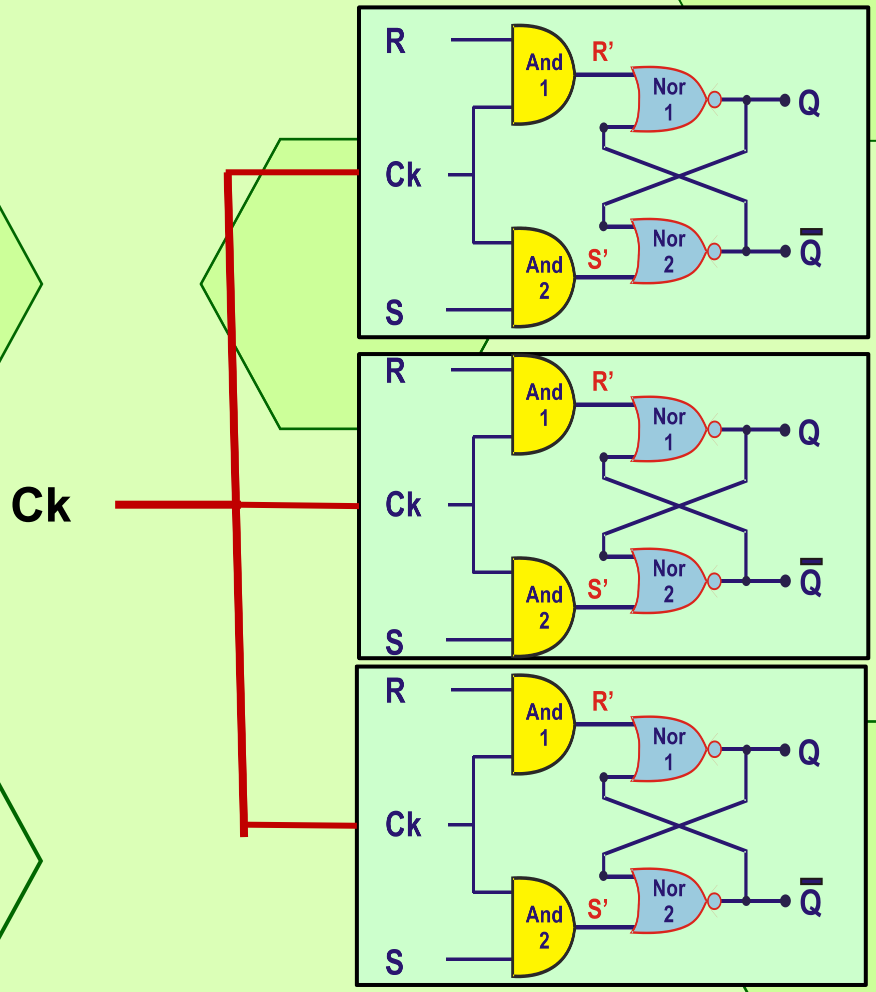


Flip Flop RS
Tabla Característica

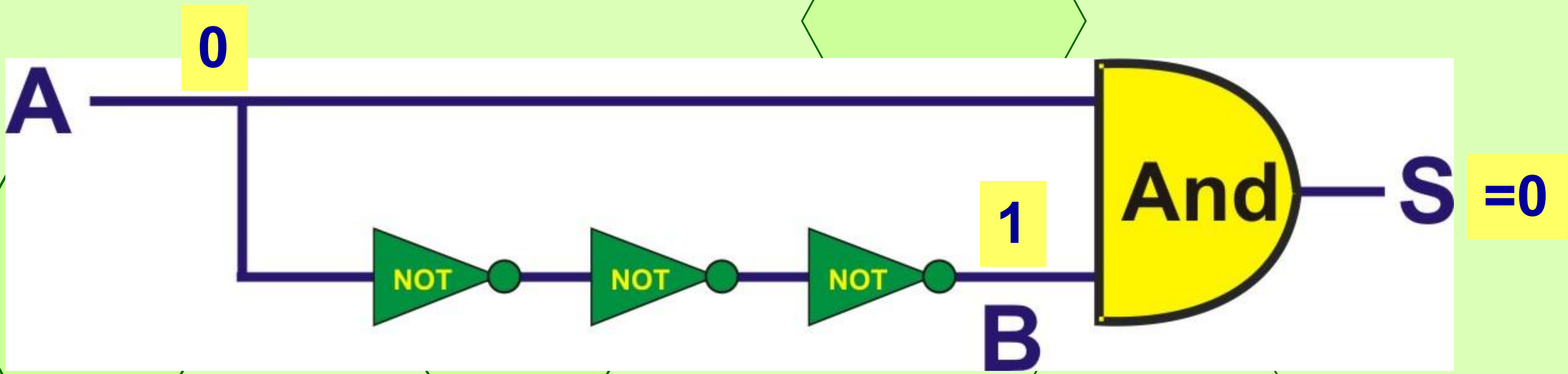
Ck	R	S	Qn+1	Q’
0	X	X	Q	Q’
1	0	0	Q	Q’
1	0	1	1	0
1	1	0	0	1
1	1	1	?	?

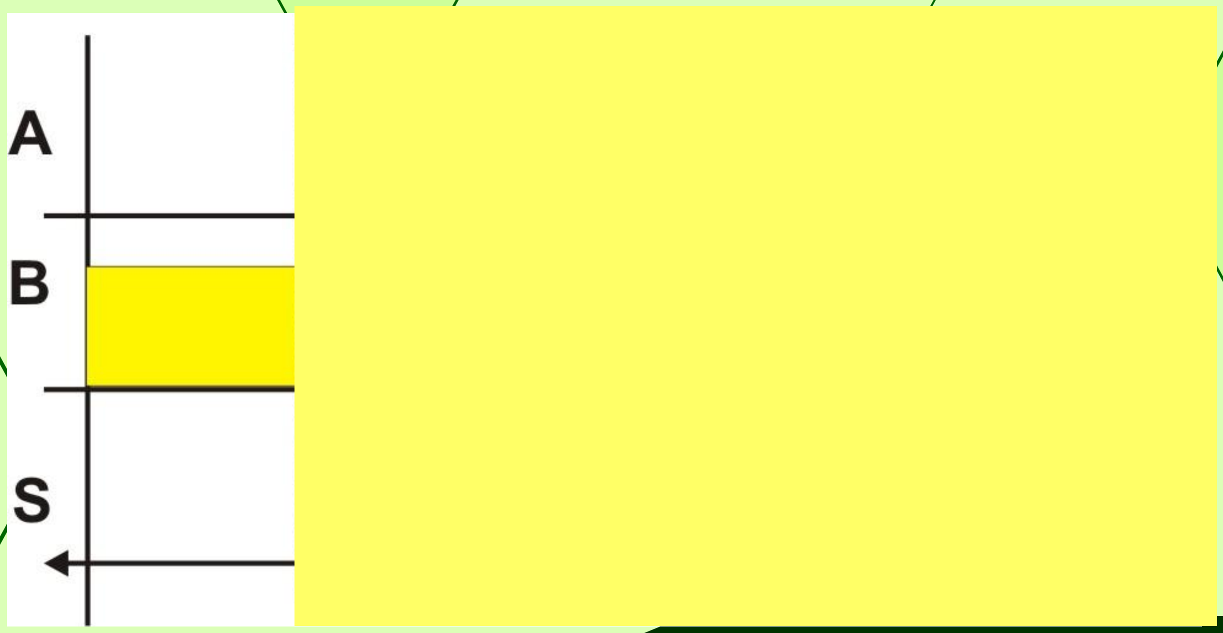


Flip Flop RS
Señal de sincronía Ck

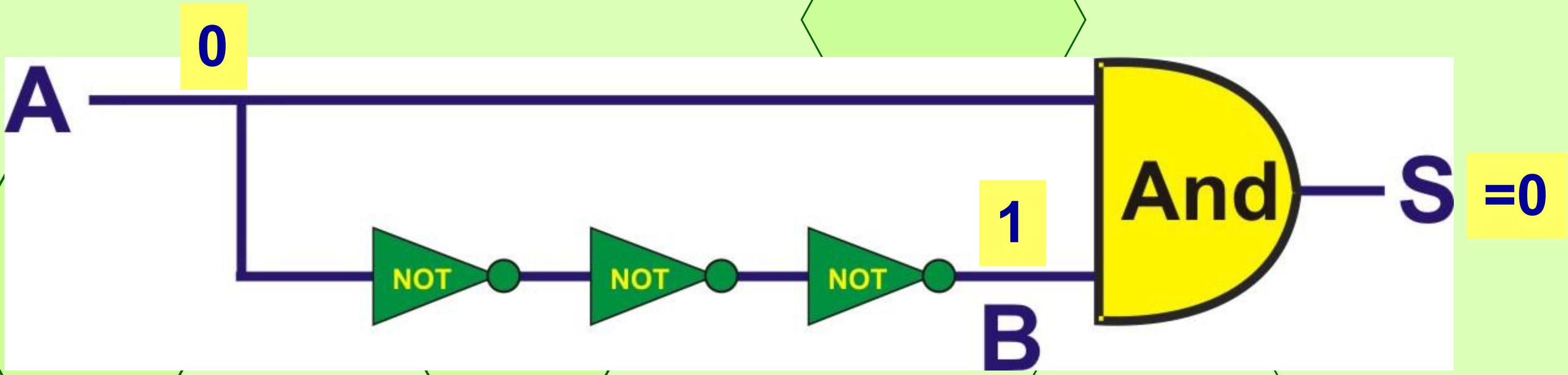


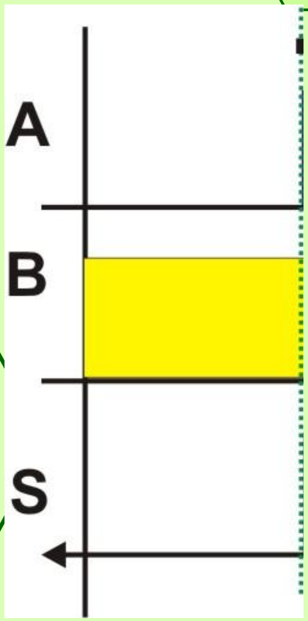
Recortador de pulso de Ck



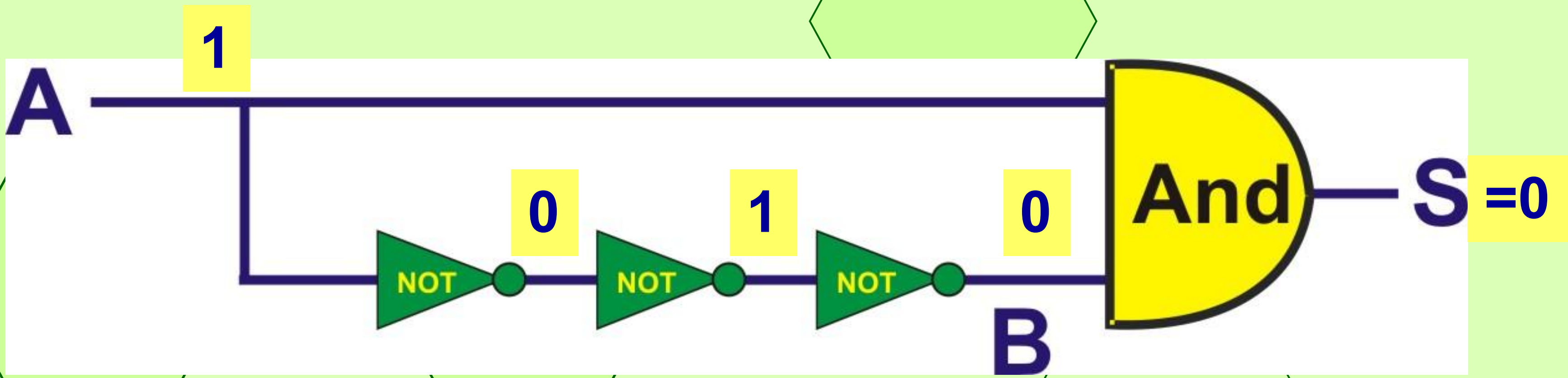


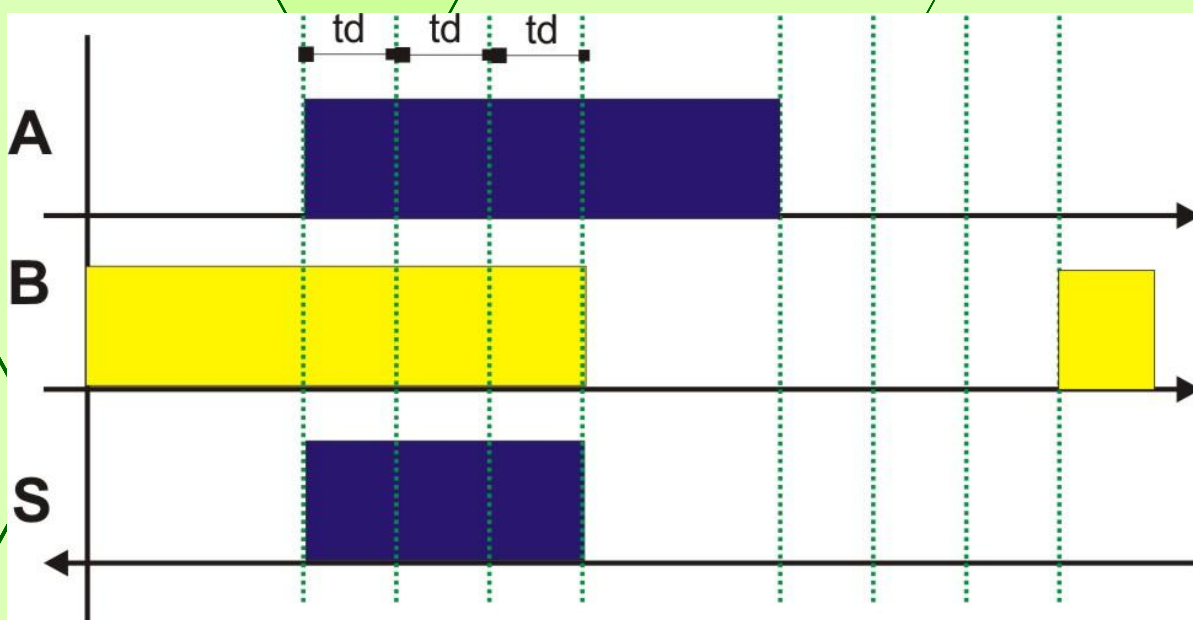
Recortador de pulso de Ck



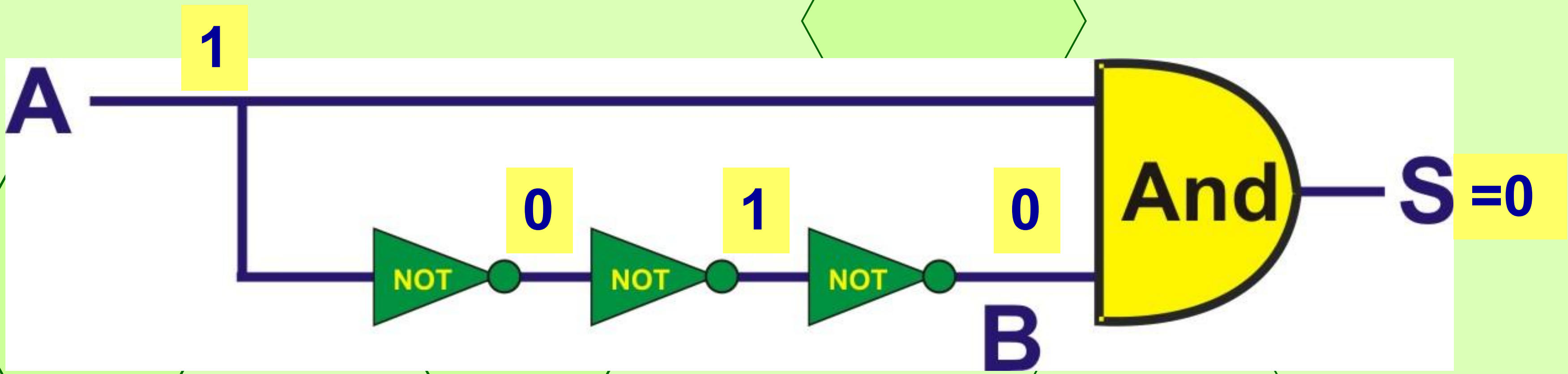


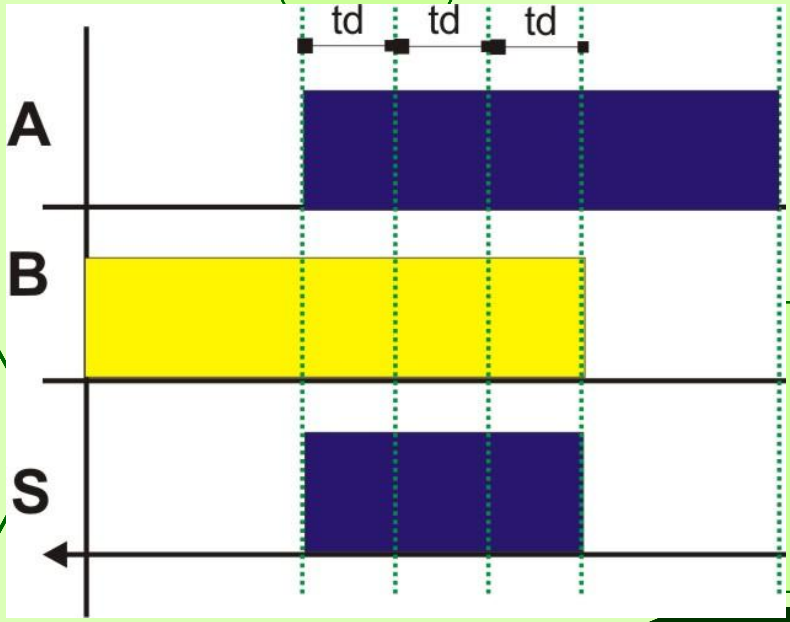
Recortador de pulso de Ck



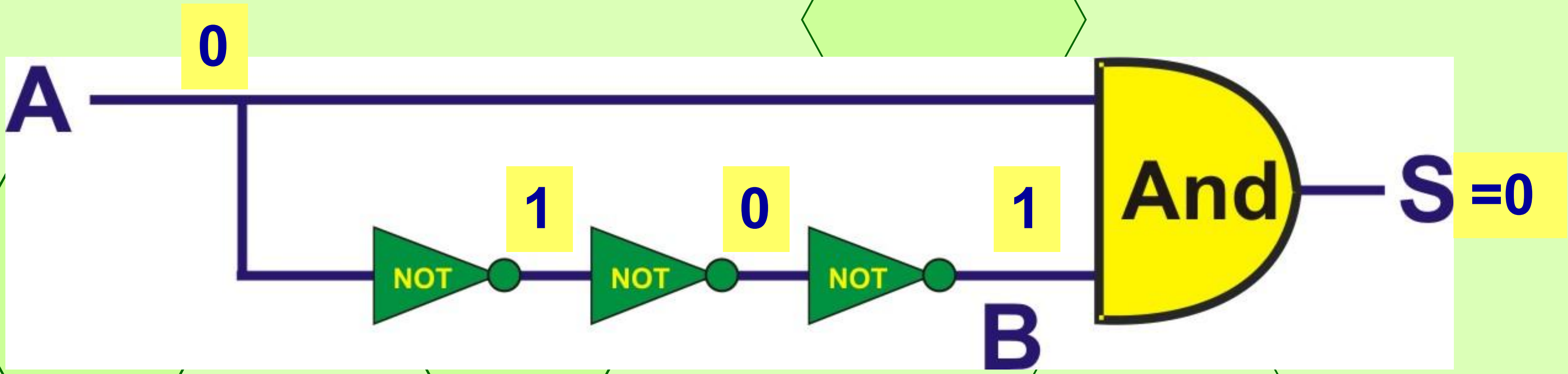


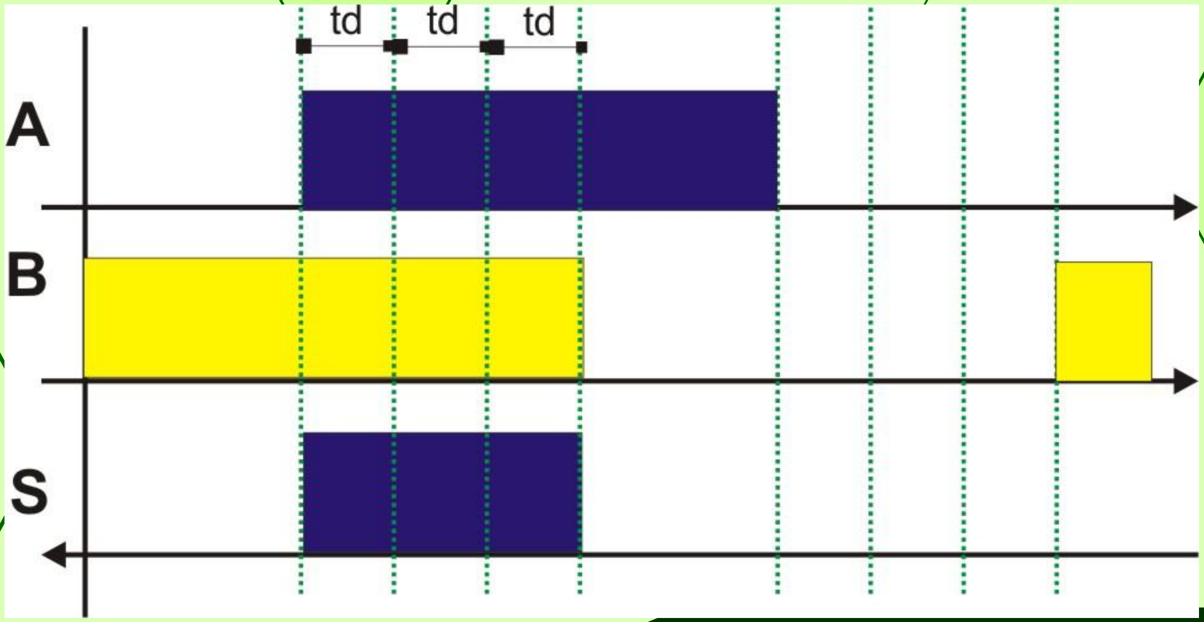
Recortador de pulso de Ck



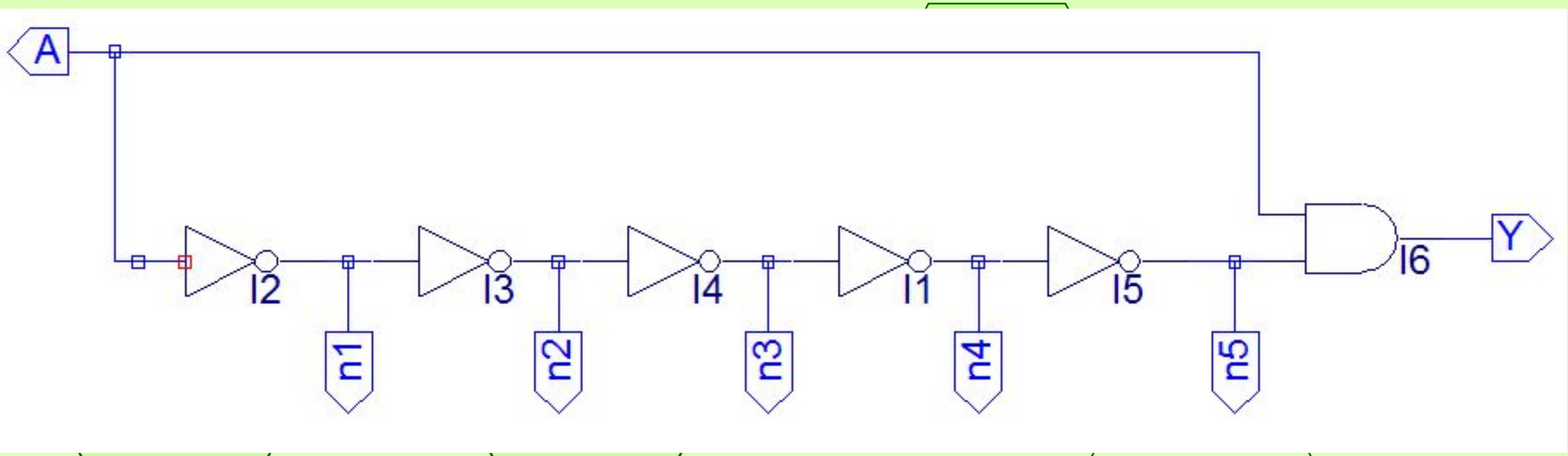


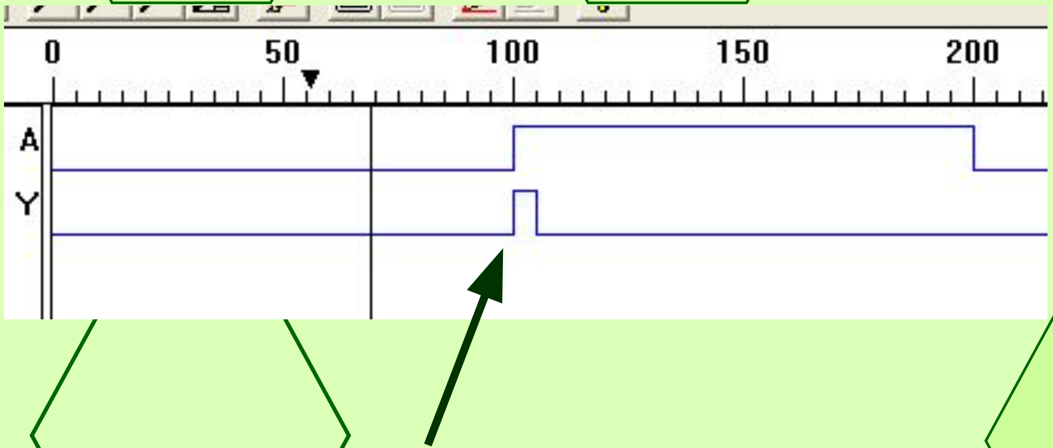
Recortador de pulso de Ck

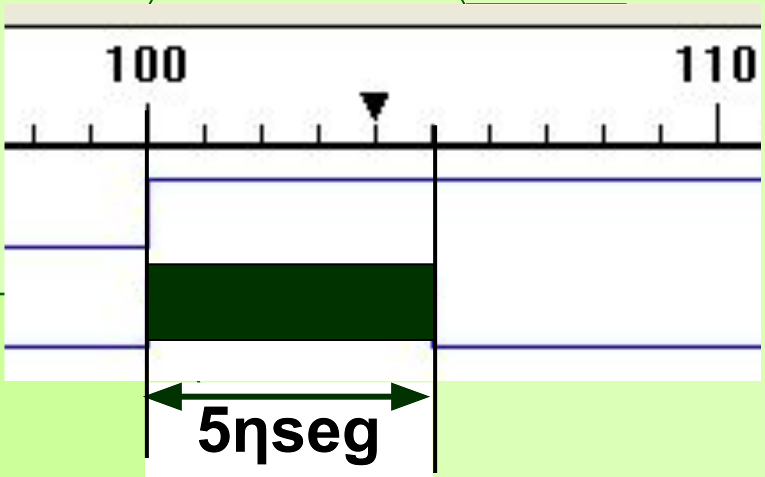




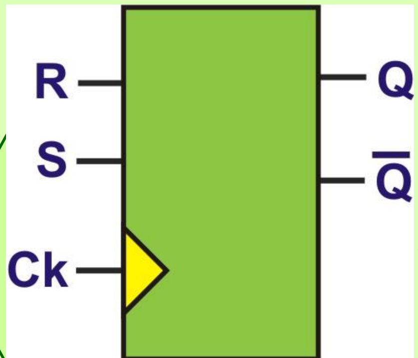
Recortador de pulso de Ck

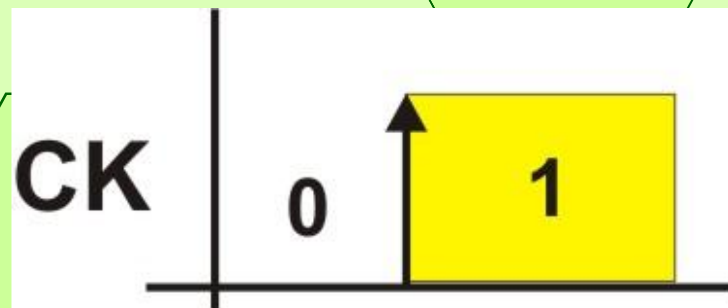




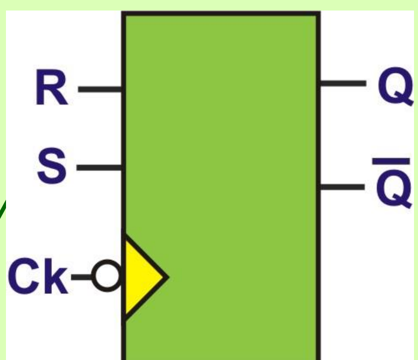


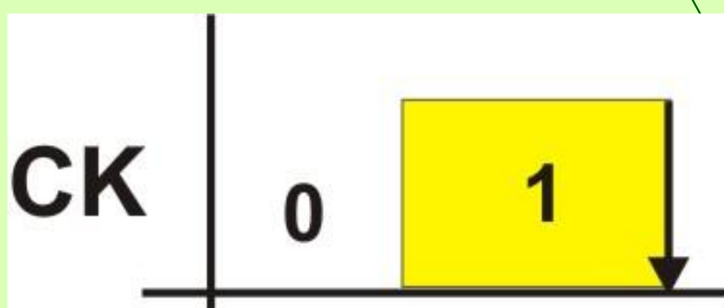
Recortador de pulso de Ck





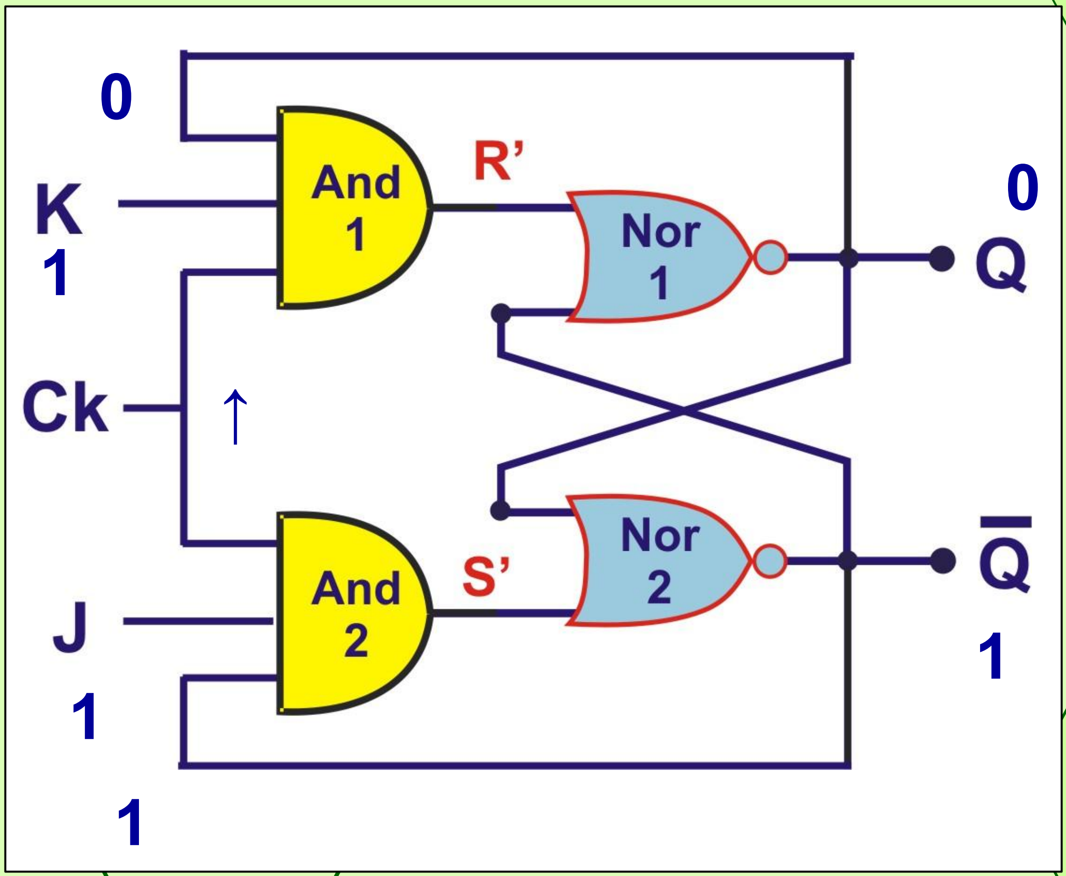
Transición Positiva



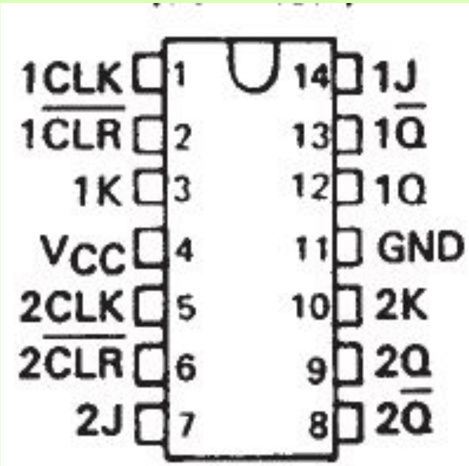


Transición Negativa

Flip Flop JK Ck ↑



Ck	J	K	Qn+1	Q'
0	X	X	Q	Q'
↑	0	0	Q	Q'
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Q'	Q



Pin Out

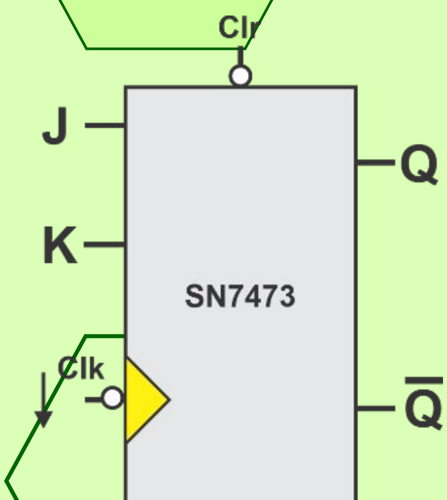
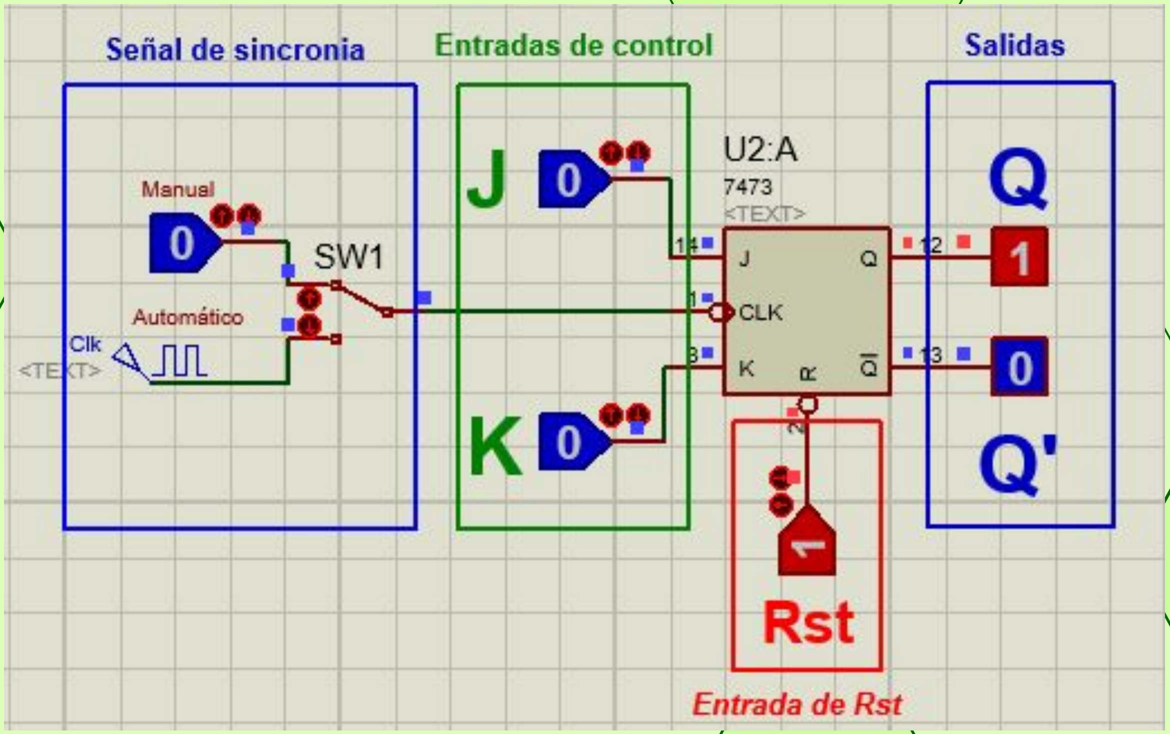


Diagrama Funcional

Entradas				Salidas	
Clr'	Clk	J	K	Q	Q'
L	X	X	X	L	H
H	↓	L	L	Q_0	Q_0'
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	Q_0'

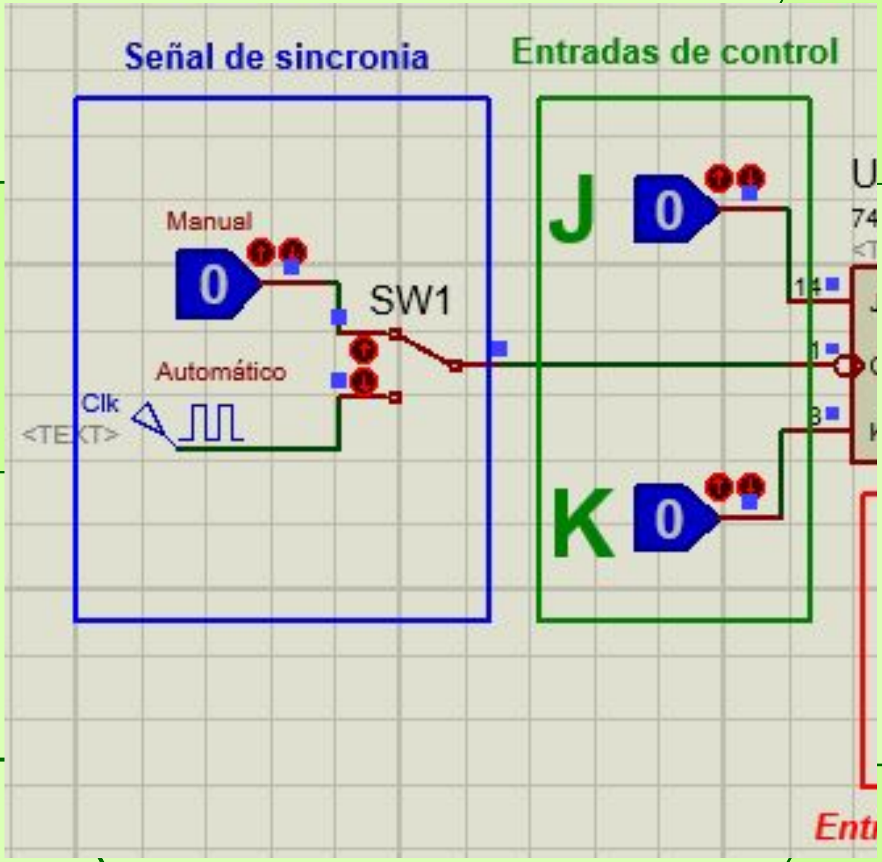
Tabla Característica

SN7473, SN74LS73 DUAL J-K FLIP-FLOPS WITH CLEAR



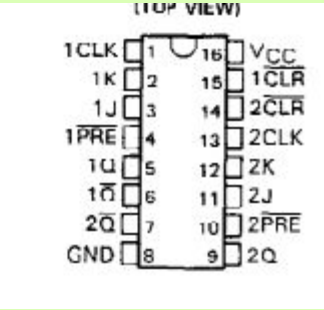
Simulación del FF JK en Proteus

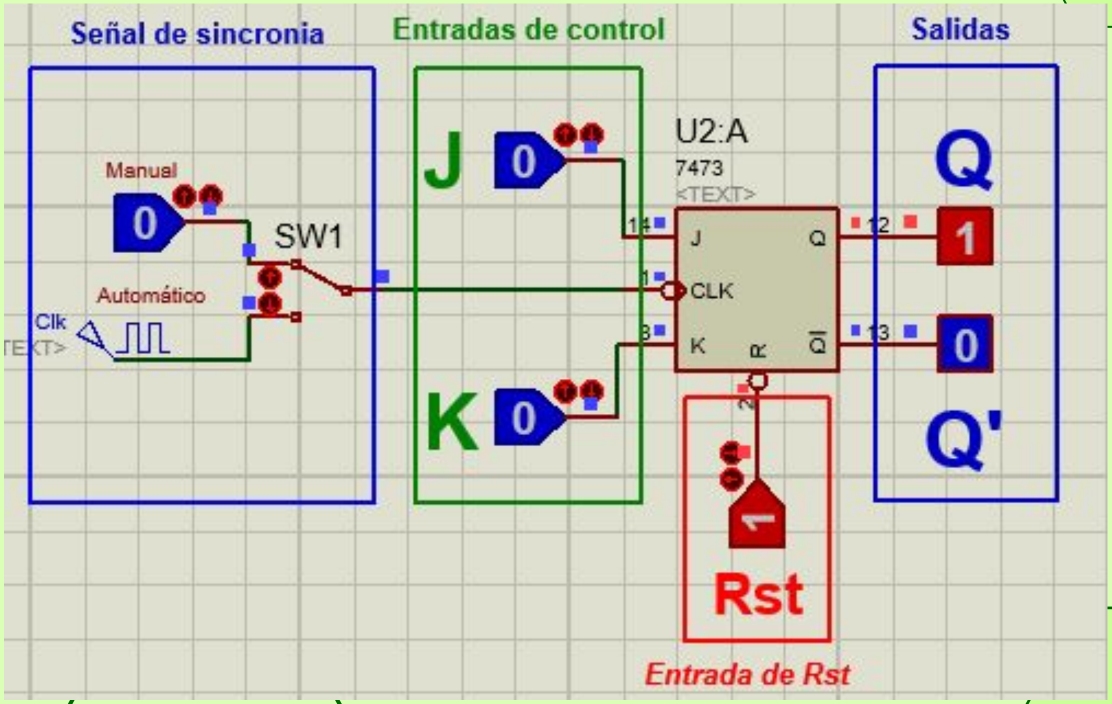
SN7473, SN74LS73 DUAL J-K FLIP-FLOPS WITH CLEAR



Simulación del FF JK en Proteus

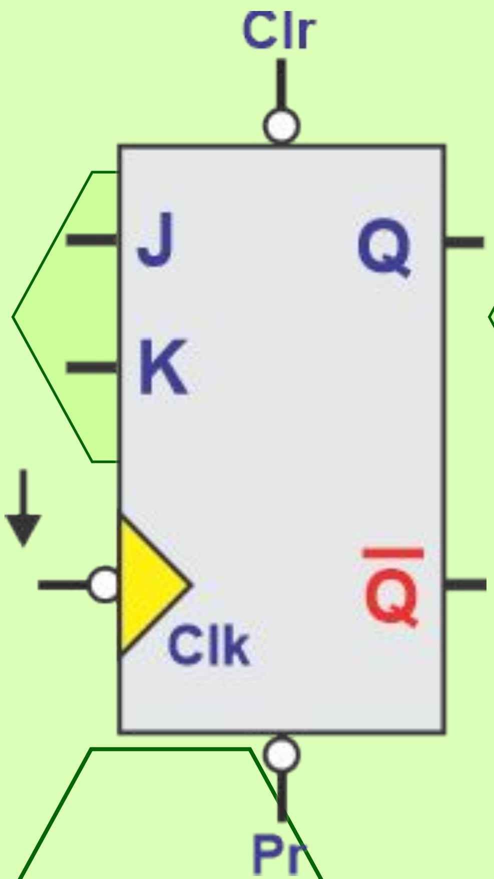
Dual J-K Flip-Flops Negative-Edge-Triggered With Preset And Clear datasheet





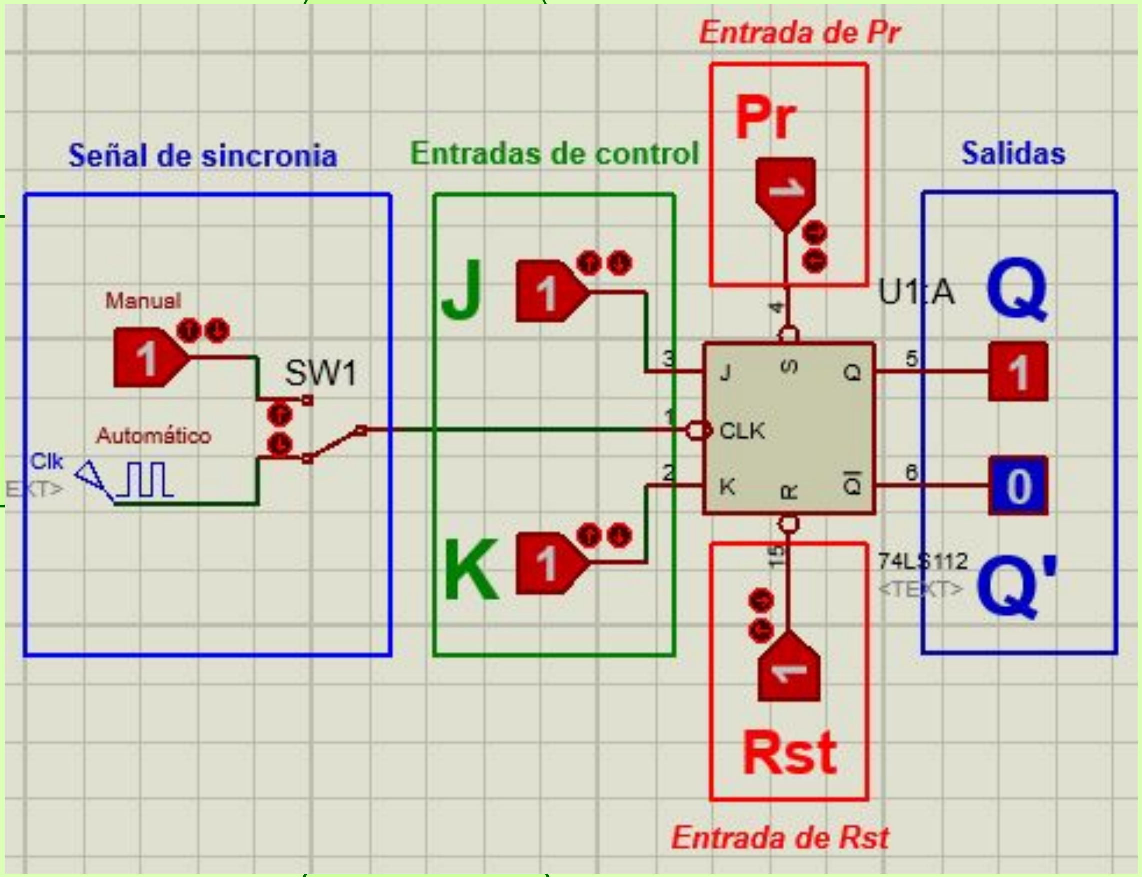
INPUTS					OUTPUTS	
PRE'	CLR'	CLK	J	K	Q	Q'
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H↑	H↑
H	H	↓	L	L	Q	Q'
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	L	X	X	Q	Q'

SN74LS112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP -FLOPS WITH PRESET AND CLEAR

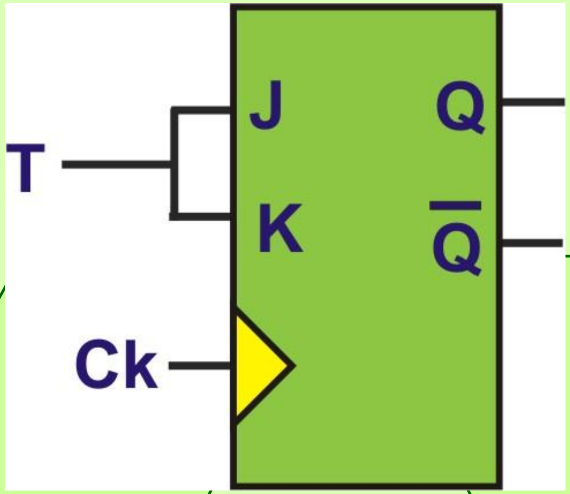


INPUTS					OUTPUTS	
Pr’	**Clr’**	**CLK**	**J**	**K**	**Q**	**Q’**
L	H	X	X	X	**H**	**L**
H	**L**	X	X	X	**L**	**H**
L	**L**	X	X	X	**H↑**	**H↑**
H	H	↓	L	L	**Q**	**Q’**
H	H	↓	H	L	**H**	**L**
H	H	↓	L	H	**L**	**H**
H	H	↓	H	H	**TOGGLE**	
H	H	L	X	X	**Q**	**Q’**

INPUTS					OUTPUTS	
Pr'	**Clr'**	**CLK**	**J**	**K**	**Q**	**Q'**
L	H	X	X	X	**H**	**L**
H	L	X	X	X	**L**	**H**
L	**L**	X	X	X	**H↑**	**H↑**
H	H	↓	L	L	**Q**	**Q'**
H	H	↓	H	L	**H**	**L**
H	H	↓	L	H	**L**	**H**
H	H	↓	H	H	**TOGGLE**	
H	H	L	X	X	**Q**	**Q'**

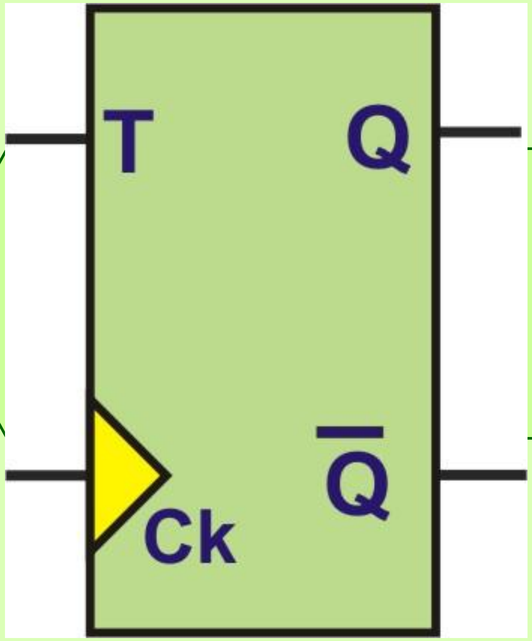


Flip Flop T
Toggle



	Ck	J	K	Qn+1	Q’
	0	X	X	Q	Q’
T=0	↑	0	0	Q	Q’
	↑	0	1	0	1
	↑	1	0	1	0
T=1	↑	1	1	Q’	Q

Ck	T	Qn+1
0	X	Q
↑	0	Q
↑	1	Q´

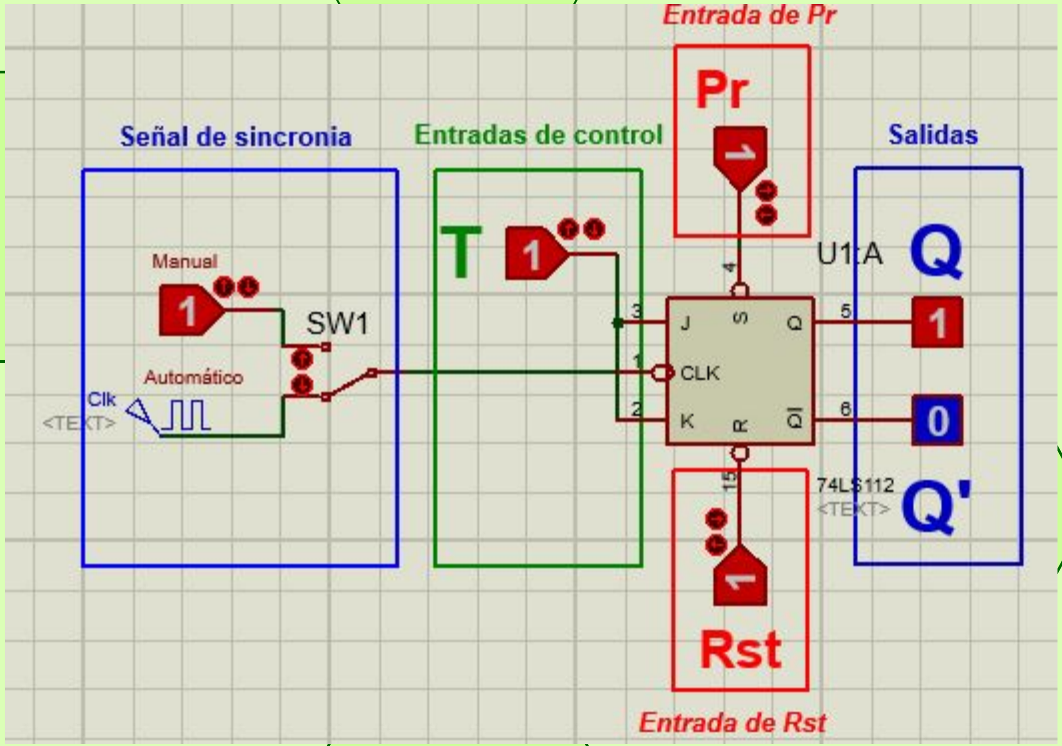


Ck	T	Qn+1
0	X	Q
↑	0	Q
↑	1	Q´

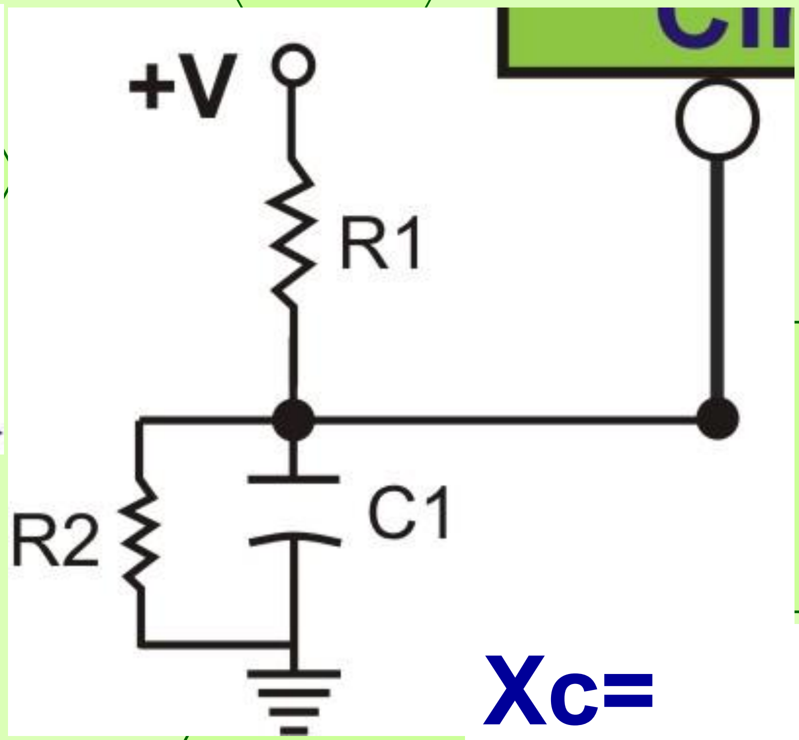
Flip Flop T
Toggle

Flip Flop T
Toggle

Rst	Ck	T	Qn+1
0	0	X	0
1	0	X	Q
1	↓	0	Q
1	↓	1	Q´

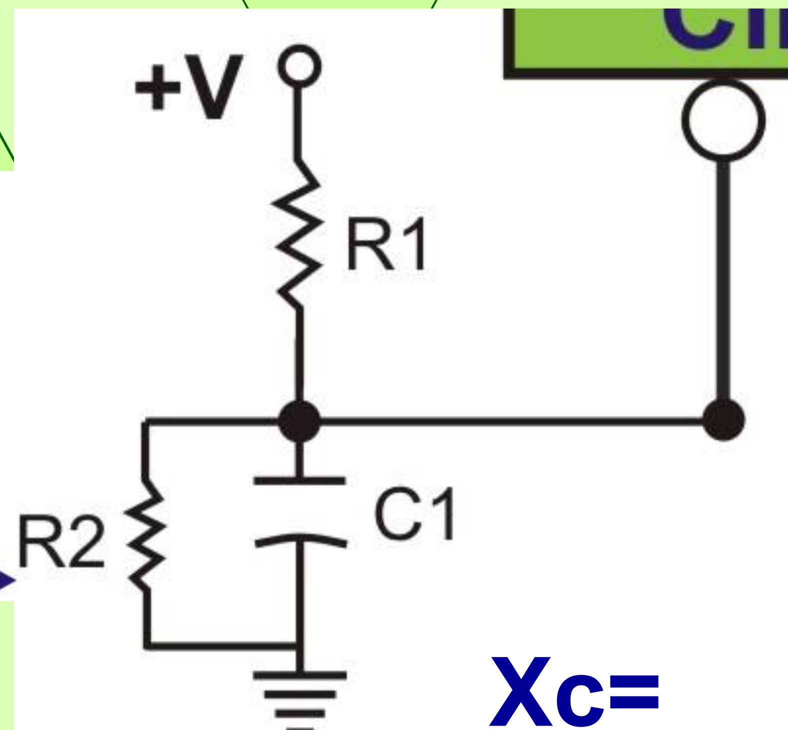


Circuito para establecer condiciones iniciales de forma automática



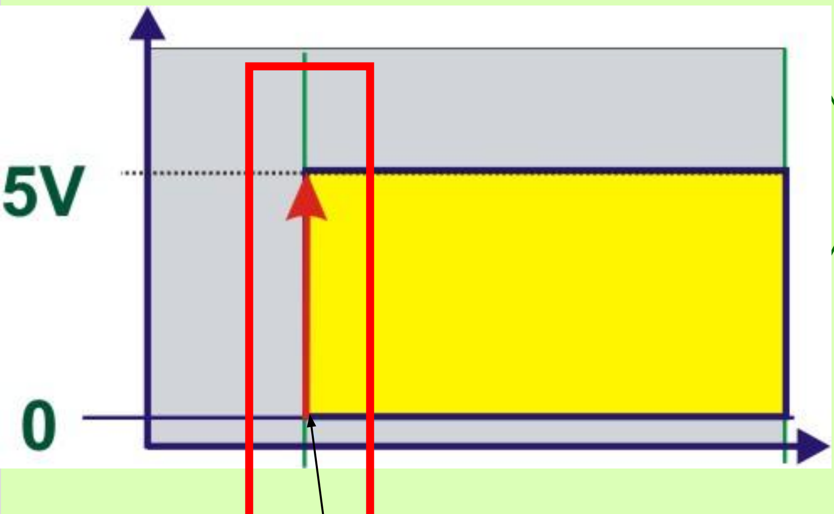
$X_c = 1/(2\pi f c)$

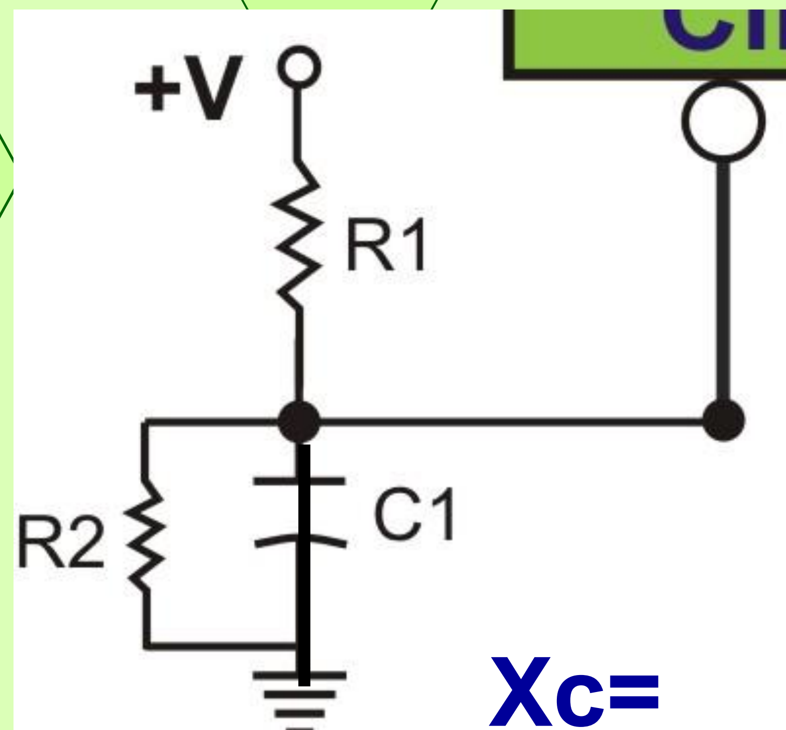
Otras entradas de Control a los FFS



Xc= 1/(2πfc)

Otras entradas de Control a los FFS



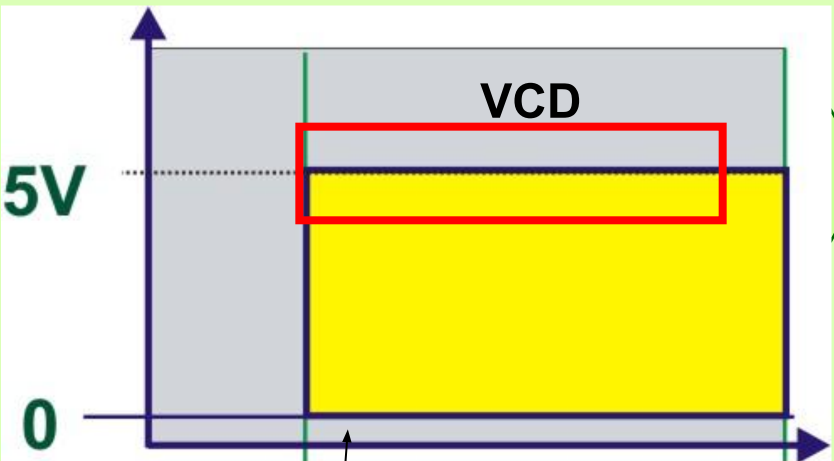


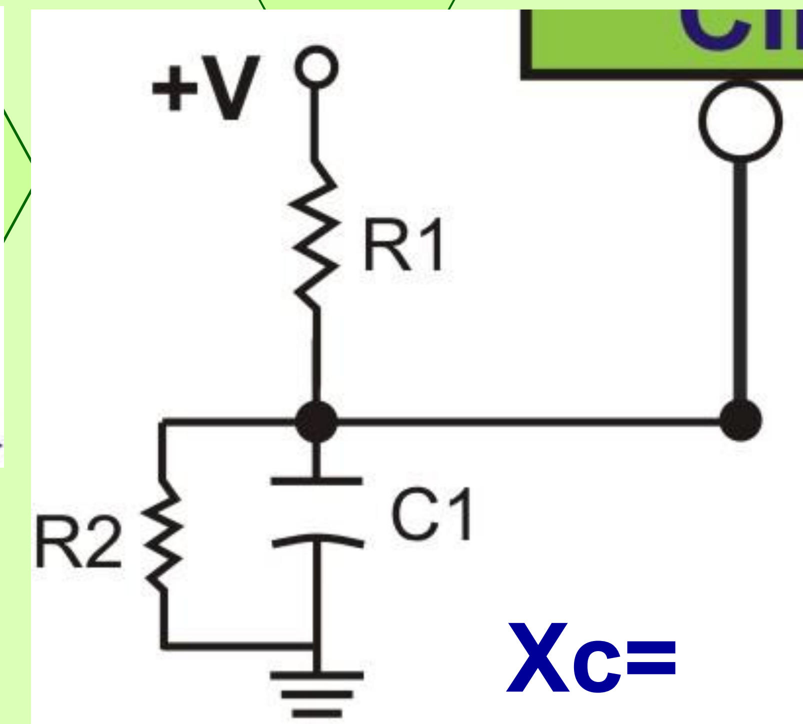
f= ∝

Xc= 1/(2πfc)

Xc= 0

Otras entradas de Control a los FFS



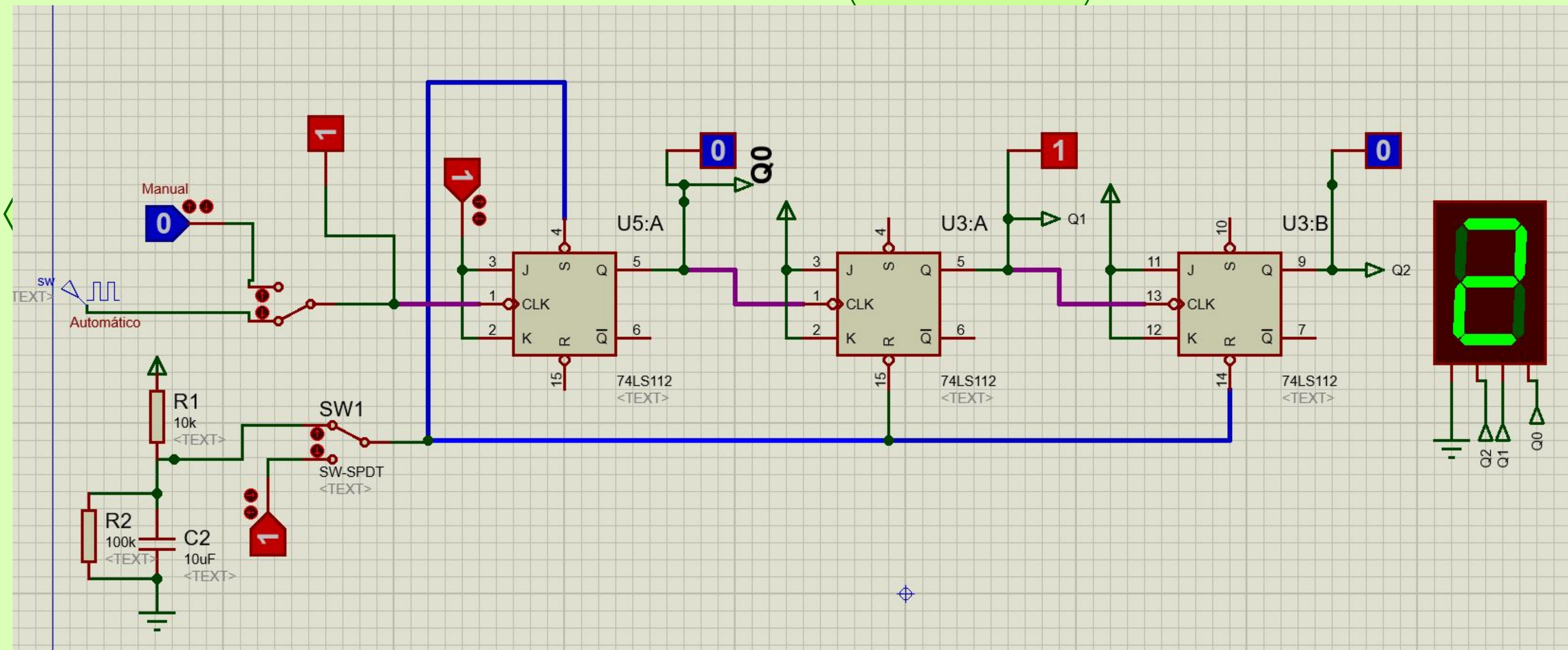


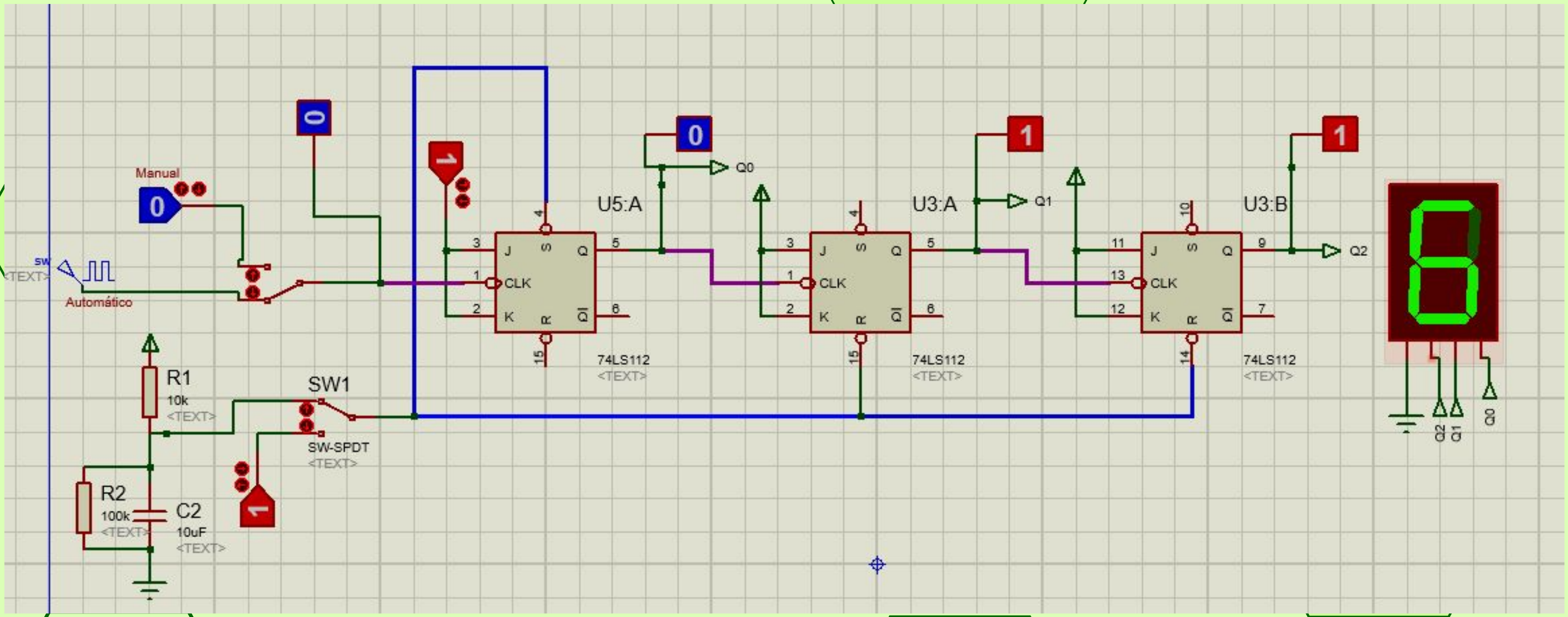
f=0

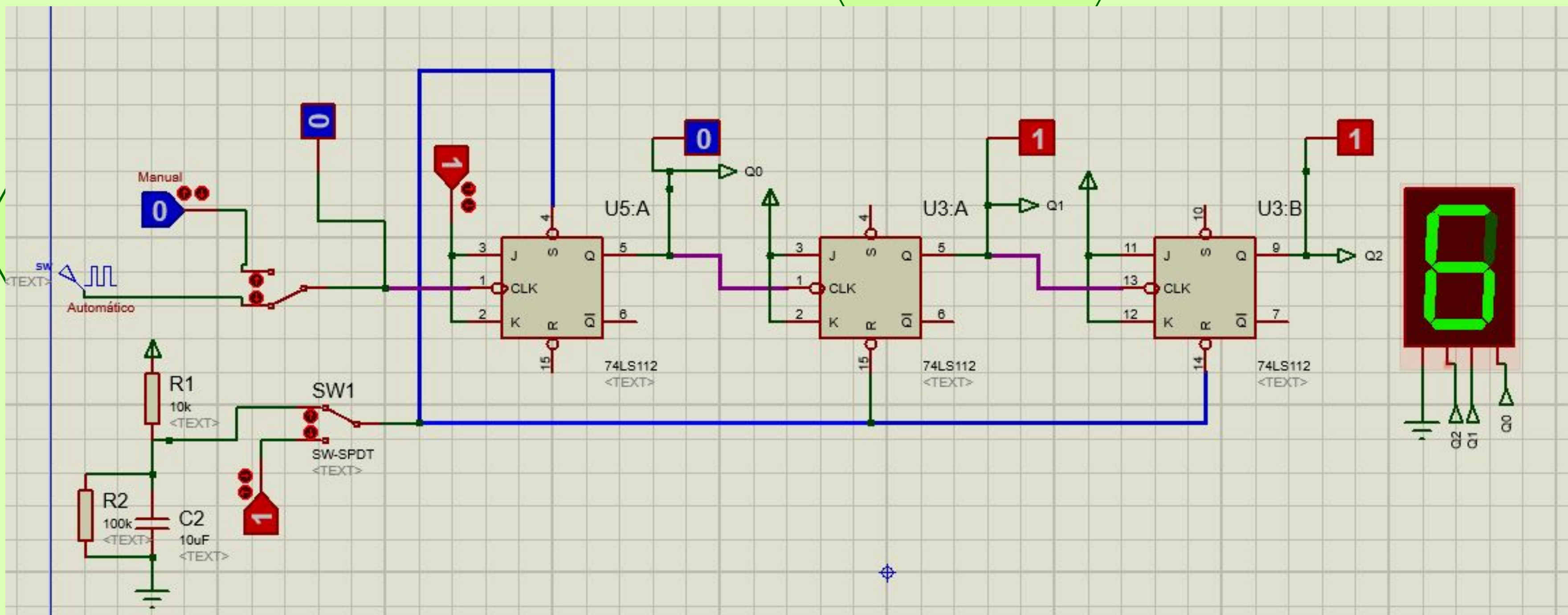
Xc= 1/(2πfc)

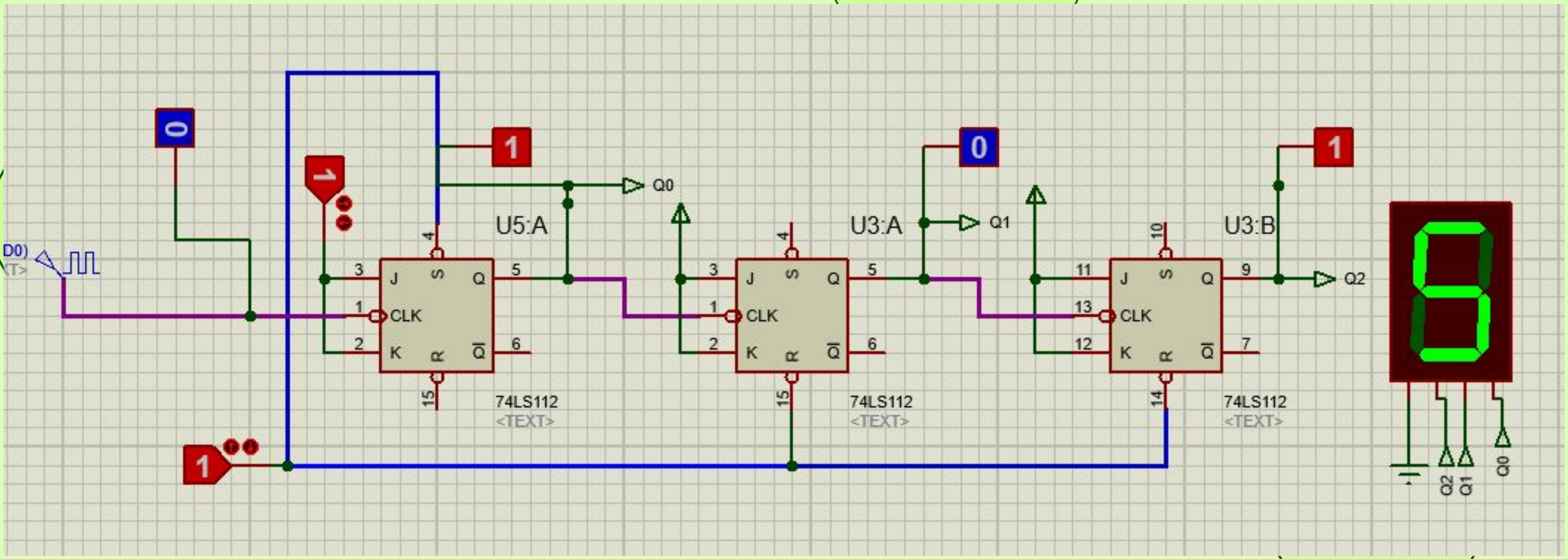
Xc= ∞

Aplicación de los FF T



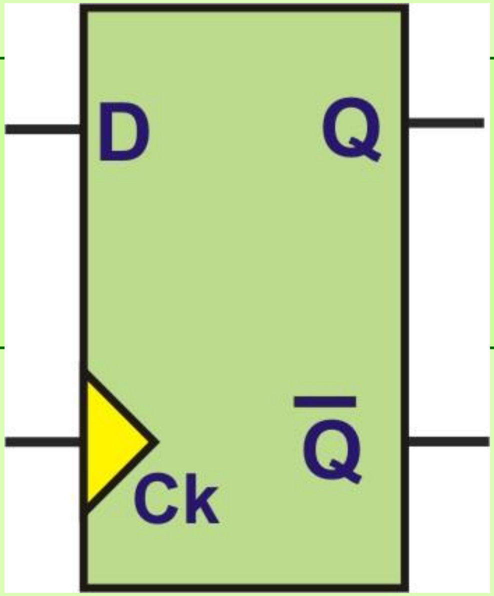

Manual
Automático
U5:A
U3:A
U3:B
74LS112
Q0
Q1
Q2
R1
10k
R2
100k
C2
10uF
SW1
SW-SPDT


Manual
Automático
U5:A
U3:A
U3:B
74LS112
74LS112
74LS112
Q0
Q1
Q2
CLK
R1
10k
R2
100k
C2
10uF
SW1
SW-SPDT


Q0
Q1
Q2
U5:A
U3:A
U3:B
74LS112
74LS112
74LS112
CLK
J
K
Q
0
1
0
1
1
1

Flip Flop D
Data

0

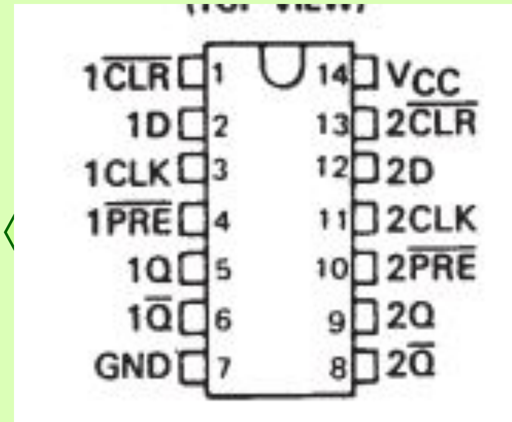


0

↑

Ck	D	Qn+1
0	X	Q
↑	0	0
↑	1	1

SN7474
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



Pin Out

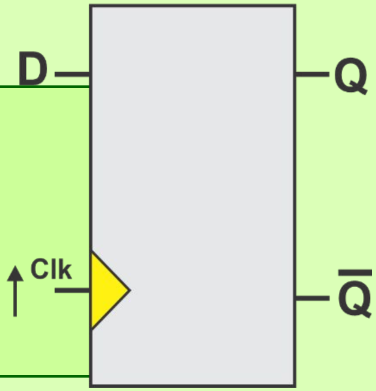
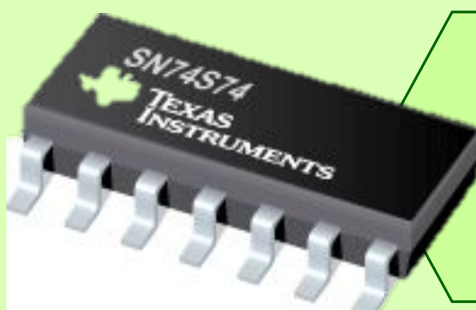


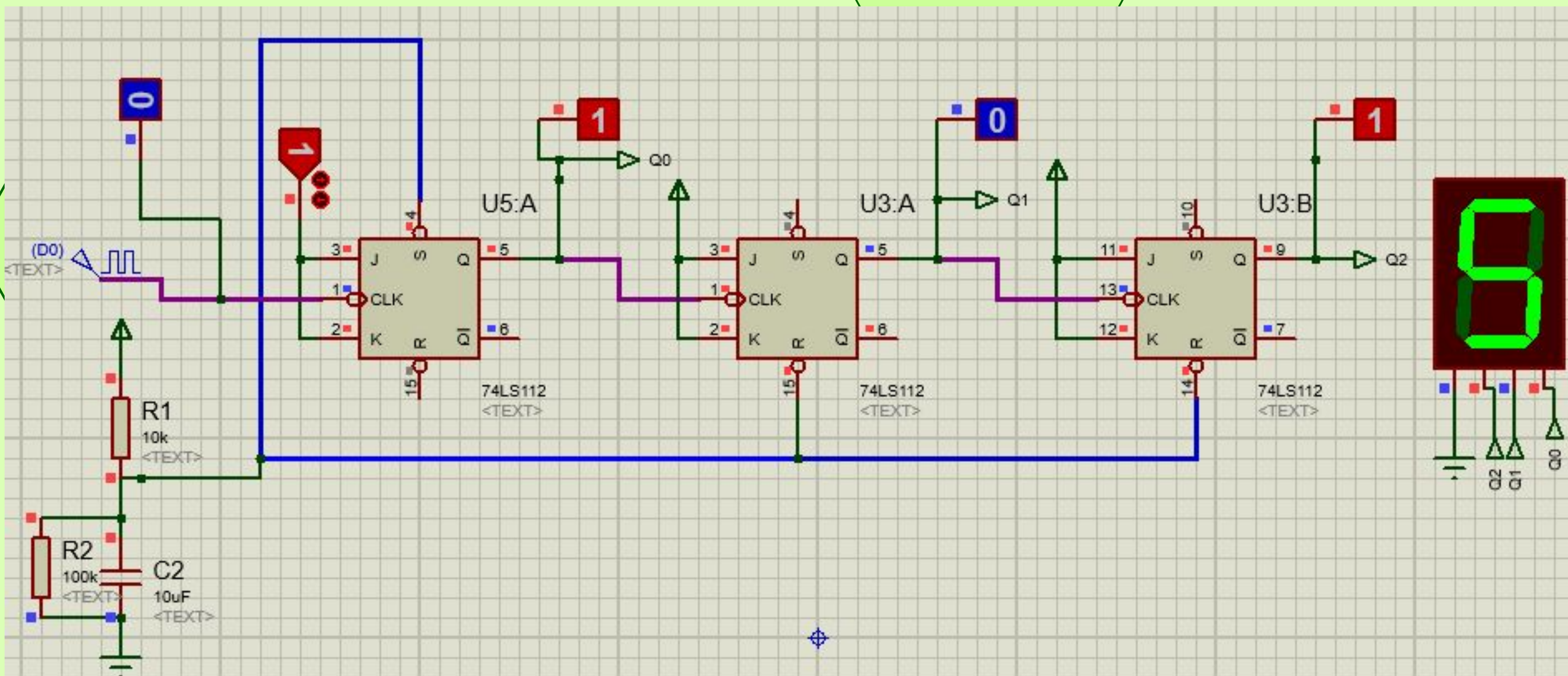
Diagrama Funcional

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Tabla Característica

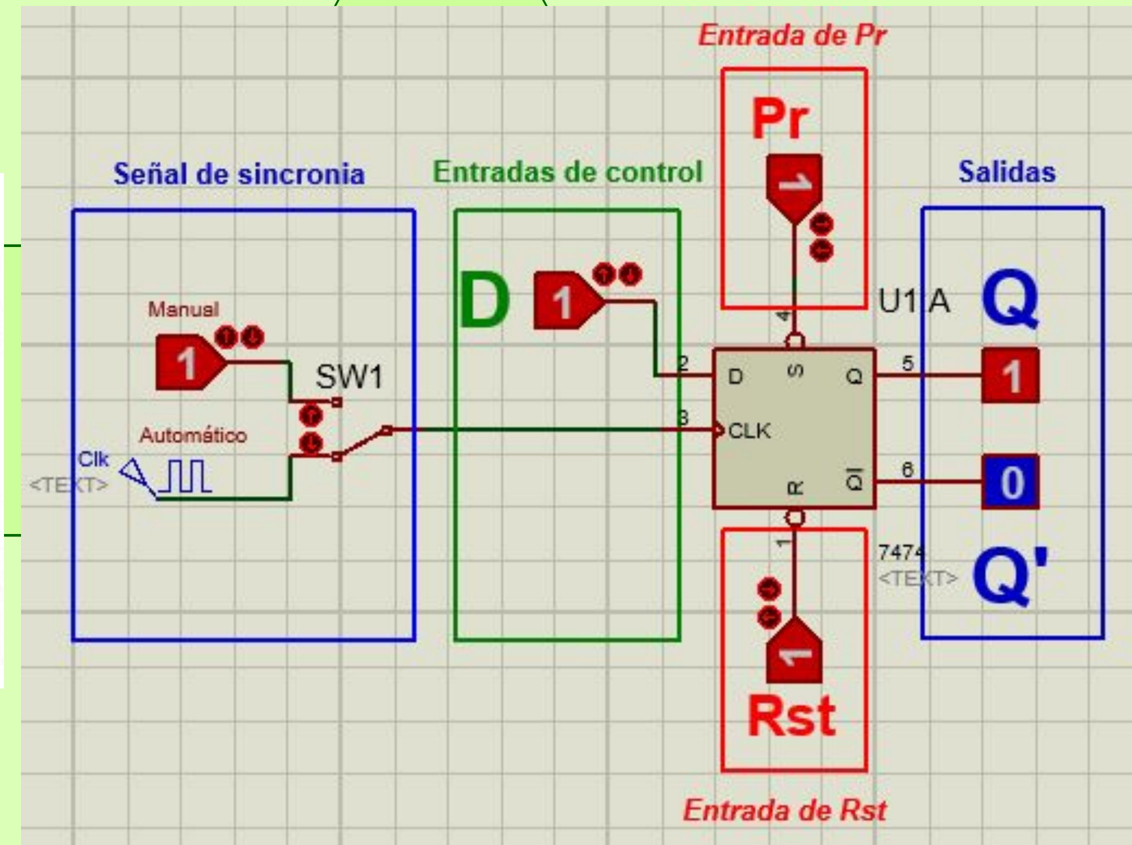


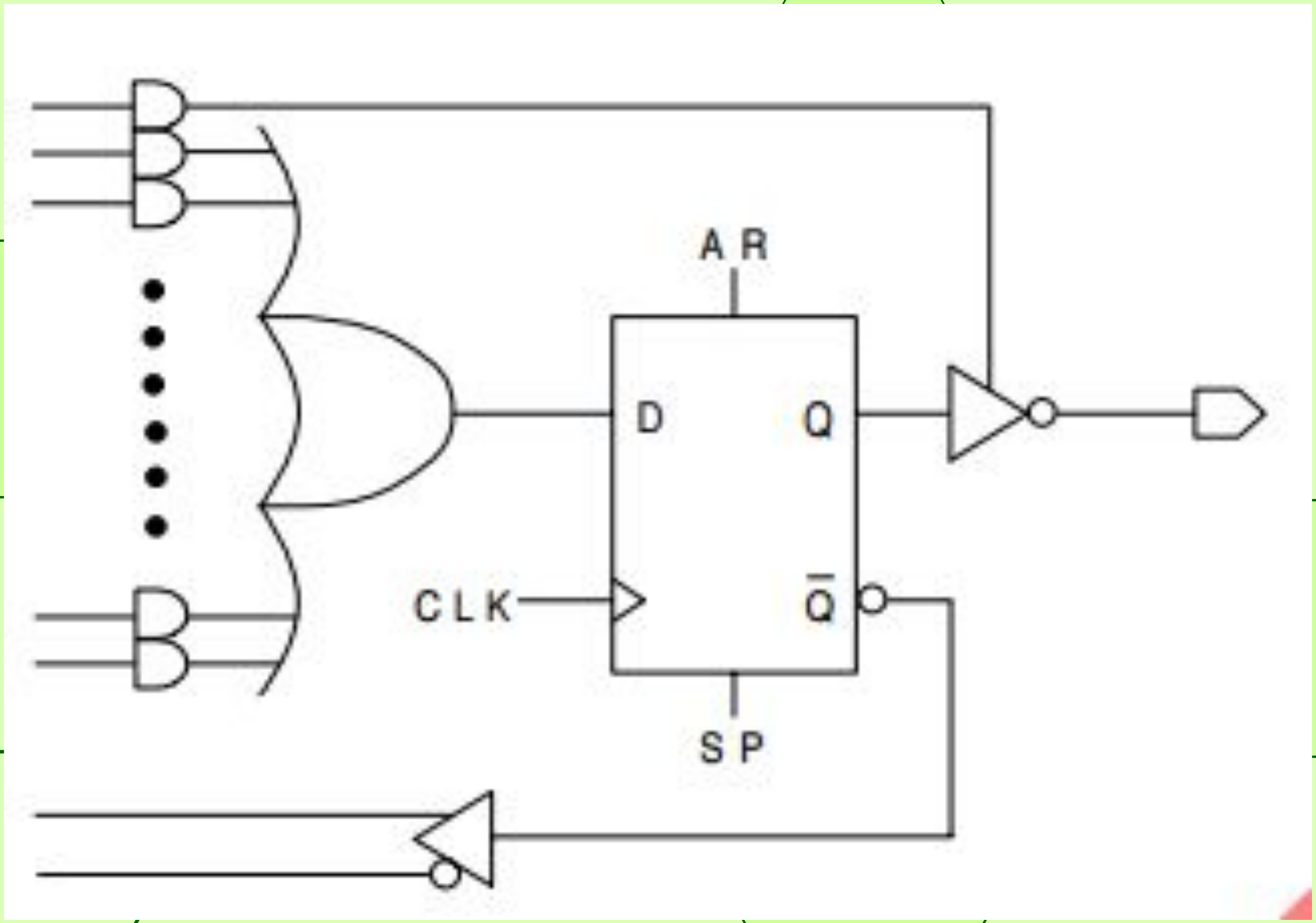

U5:A
U3:A
U3:B
74LS112
74LS112
74LS112
Q0
Q1
Q2
R1
10k
R2
100k
C2
10uF
(D0)
CLK
J
K
Q

FF D

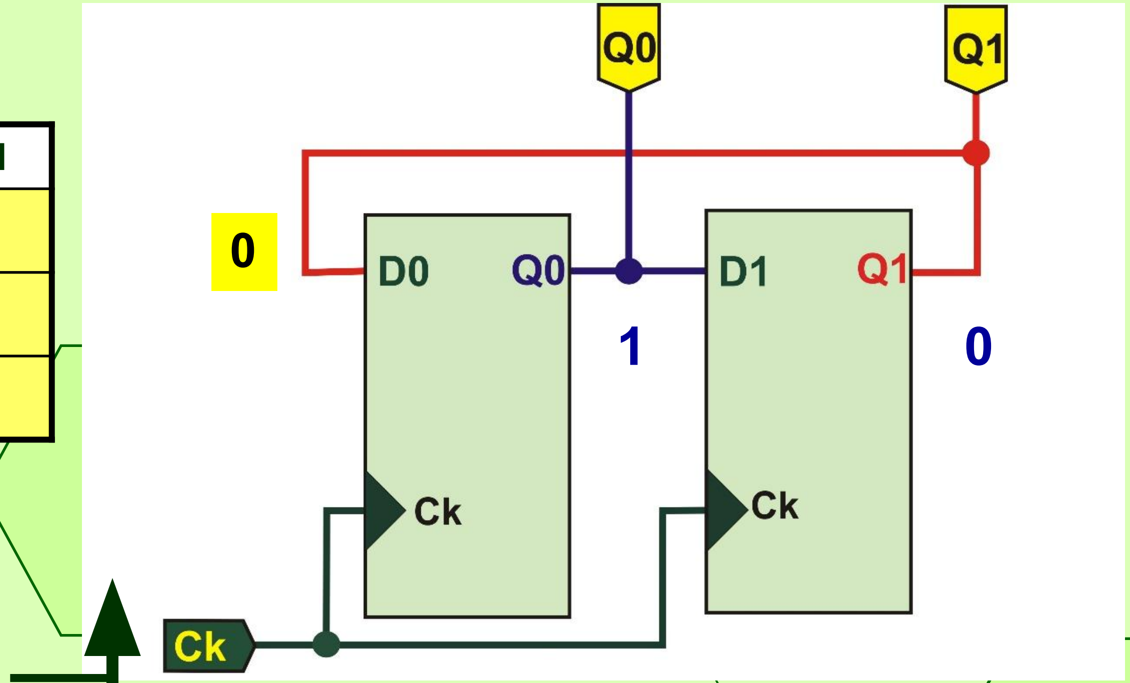
FUNCTION TABLE

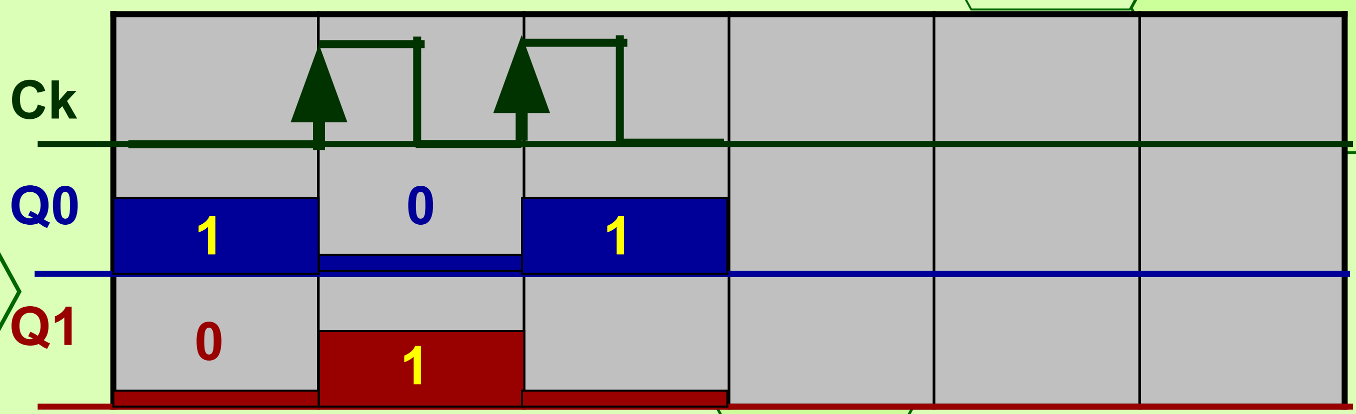
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

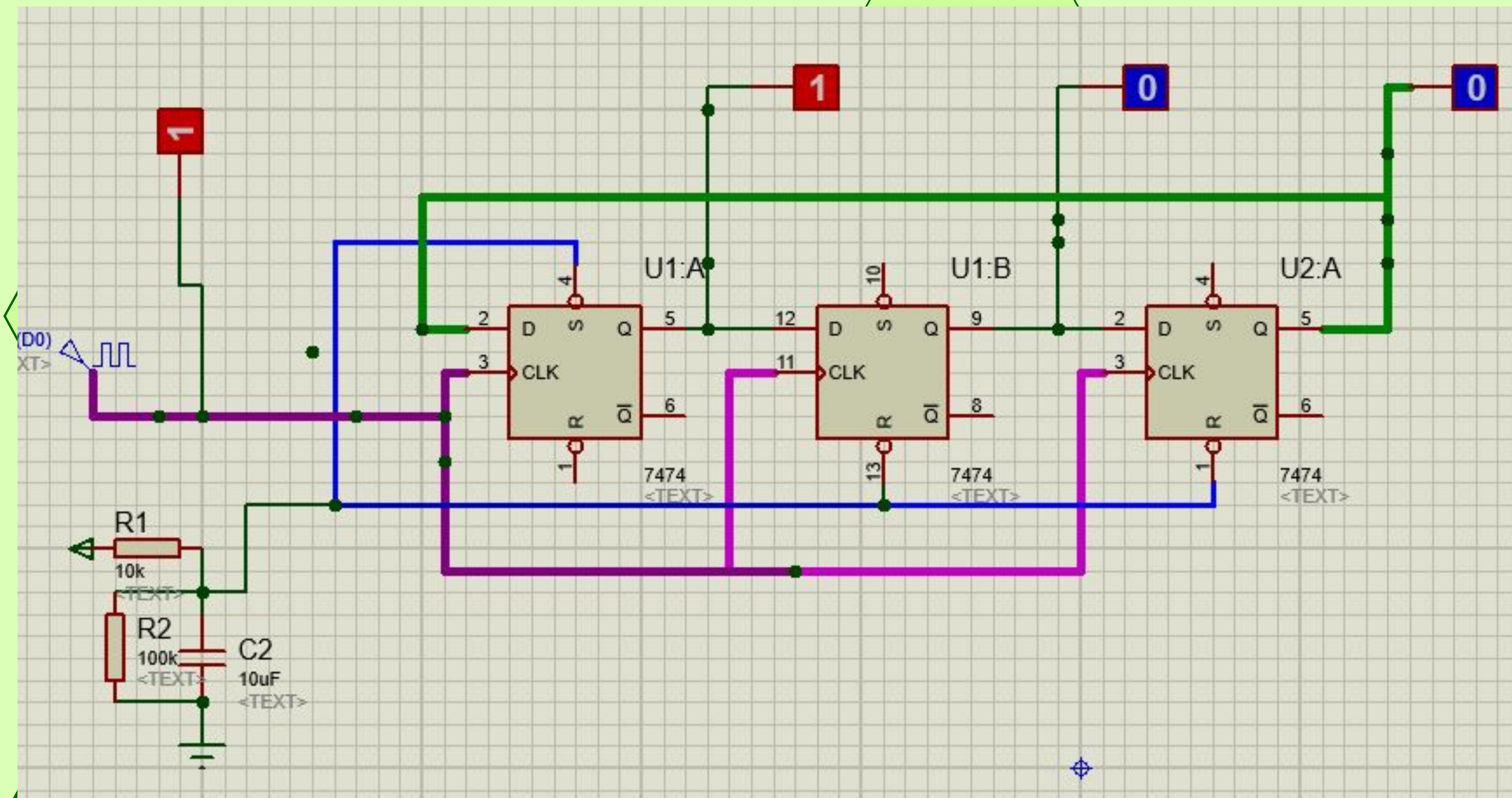



A R
D
Q
C L K
$\bar{Q}$
S P

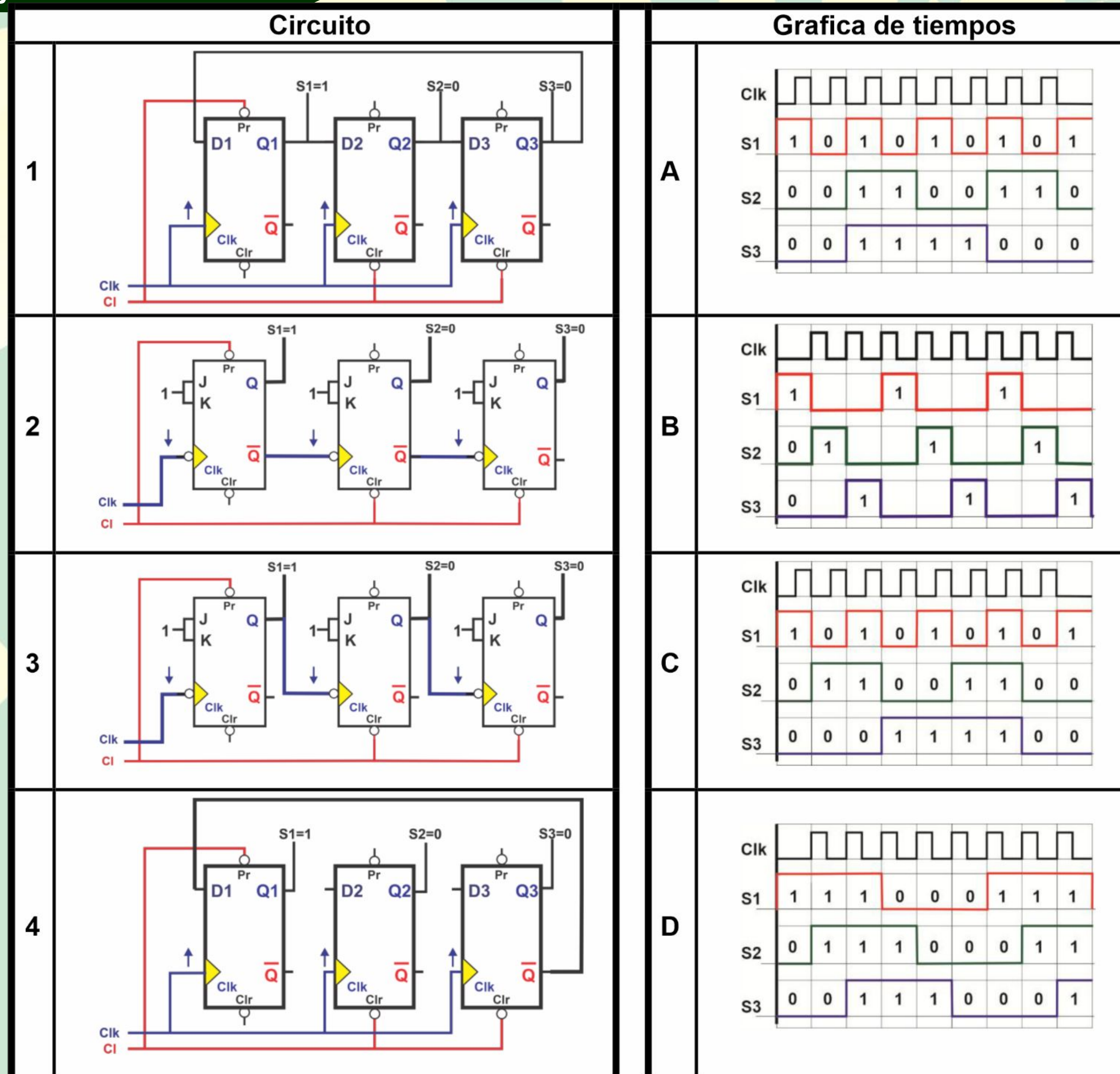
Ck	D	Qn+1
0	X	Q
↑	0	0
↑	1	1






1
1
0
0
U1:A
U1:B
U2:A
D
CLK
Q
S
R
7474
<TEXT>
R1
10k
R2
100k
C2
10uF

Proyecto Formativo 9



- **Concepto de Memoria**
- **Tipos de Flip Flops**
- **Clk** (sincronía)
  - Manual
  - Automática
- Otras entradas de control **Clr**, **Pr**
- Establecer condiciones iniciales al arranque
- Algunas aplicaciones de los FF´s